Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY
BE SEM-VI Examination-Nov/Dec-2011

Subject code: 161004 **Date: 28/11/2011**

Subject Name: VLSI Technology and Design

Time: 10.30 am -1.00 pm **Total marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain the fabrication steps of nMOS transistor with necessary figures. **07**

(b) Explain VLSI Design flow using Y-chart. **07**

Q.2 **(a)** Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA). **07**

(b) Consider a MOS system with the following parameters: **07**

$t_{ox} = 200$ Å

$\varphi_{GC} = -0.85$ V

$N_A = 2 \times 10^{15}$ cm^{-3}

$Q_{ox} = q \times 2 \times 10^{11}$ C/cm^2

Determine the threshold voltage VTO under zero bias at room temperature. Note that $\varepsilon_{ox} = 3.97\varepsilon_0$ and $\varepsilon_{si} = 11.7\ \varepsilon_0$.

OR

(b) Design a resistive load inverter with R = 1kΩ, such that $V_{OL} = 0.6$V. The enhancement-type nMOS driver transistor has the following parameters: **07**

$V_{DD} = 5.0$V

$V_{TO} = 1.0$ V

$\gamma = 0.2$ V$^{1/2}$

$\lambda = 0$

$\mu_n C_{ox} = 22.0\ \mu$A/V^2

a. Determine the required aspect ratio, W/L.

b. Determine V_{IL} and V_{IH}.

Q.3 **(a)** Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} and V_{IL} for depletion- load nMOS inverter. **07**

(b) Explain two input depletion load NOR gate and derive the necessary equations for the same. **07**

OR

Q.3 **(a)** Write a note on CMOS Ring Oscillator circuit. **07**

(b) Implement CMOS clocked JK latch. **05**

(c) Realize the following Boolean function using CMOS TG. **02**
F = AB + A'C' + AB'C.

Q.4 **(a)** Explain the basic principle of pass transistor circuit. Explain logic "1" transfer and logic "0" transfer. **07**

	(b)	Draw input and output waveforms during high to low transition of output for a CMOS inverter. Derive expression for τ_{PHL}.	**07**

OR

Q.4	**(a)**	Draw the circuit diagram of Domino CMOS logic gate and discuss it in detail.	**07**
	(b)	Explain latch-up problem in CMOS inverter. Discuss causes for latch-up.	**07**
Q.5	**(a)**	List Ad-hoc testable design techniques and discuss any two in detail.	**07**
	(b)	Implement the following Boolean function using CMOS. F =[(C+D+E) . (B+A)]'. Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that (W/L)p = 15 for all pMOS transistors and (W/L)n = 10 for all nMOS transistors.	**07**

OR

Q.5	**(a)**	Write a short note on Built In Self Test (BIST).	**07**
	(b)	Give comparison between FPGA and CPLD.	**07**

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