Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

BE Sem-VI Summer Exam 2012

Subject code: 161004 Subject Name: VLSI Technology and Design

Date:17/05/2012 Total Marks: 70 Time duration:10:30am to 1.00pm

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following: **07**

(I) Compare Semi-custom and Full custom VLSI design style

(II) Discuss general architecture of FPGA

(b) Discuss process flow for the fabrication of an n-type MOSFET on p-type silicon **07**

Q.2 **(a)** Answer the following: **07**

(I) Implement following Boolean functions

$F = BC + \bar{B}\bar{A} + B\bar{C}A$ using transmission gates

(II) Draw the Gate level schematic and CMOS Implementation of D-latch:

(b) Define and discuss Latch-up problem in CMOS inverter. Mention causes for latch-up and guideline for avoiding latch-up. **07**

OR

(b) Discuss Ad Hoc testable design techniques **07**

Q.3 **(a)** Draw the CMOS Inverter circuit and Voltage Transfer Characteristic (VTC) for different operating regions of the nMOS and pMOS transistors. Derive critical voltage points V_{IL},V_{IH}. **07**

(b) Consider a CMOS Inverter circuit with the following parameters: **07**
V_{DD}=3.3V, $V_{TO,n}$=0.6V , $V_{TO,p}$= - 0.7V, k_n=200 $\mu A/V^2$, k_p=80 $\mu A/V^2$
Calculate the noise margin of the circuit.

OR

Q.3 **(a)** Explain Band Diagram of the MOS structure, at surface Inversion. Derive the expression of threshold Voltage. **07**

(b) Calculate the threshold voltage V_{TO} at V_{SB} = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox}=500 Angstrom and oxide interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}, ϕ_F(gate) = 0.55V. Physical constants : **07**
Thermal voltage =KT/q = 0.026 volt
Energy Gap of silicon(Si) =Eg = 1.12 eV
Intrinsic Carrier Concentration of silicon = ni =1.45×10^{10} cm^{-3}
Dielectric constant of vaccume = $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm
Dielectric constant of silicon = $\varepsilon_{si} = 11.7 \times \varepsilon_o$ F/cm
Dielectric constant of silicon dioxide = $\varepsilon_{ox} = 3.97 \times \varepsilon_o$ F/cm

Q.4 **(a)** Draw input and output waveform during high to low transition of output for a CMOS inverter and derive expression for τ_{PHL} **07**

(b) What is the need of voltage bootstrapping? Discuss Voltage bootstrapping in detail. **07**

OR

Q.4 **(a)** Discuss procedure to measure data for experimental determination of the parameters $k_{n,}$ V_{TO} and substrate bias coefficient. **07**

(b) Draw and discuss three stage ring oscillator circuit. **07**

Q.5 **(a)** Discuss dynamic CMOS logic (precharge – evaluate logic) with illustration of the cascading problem in dynamic CMOS logic. **07**

(b) Define or briefly discuss following: **07**

1. Narrow channel effect
2. Observability in testing
3. Causes for chip reliability
4. Negative photoresist
5. Need of H-tree Clock distribution network
6. Power delay product
7. Need of Domino CMOS logic

OR

Q.5 **(a)** Derive equivalent resistance of the CMOS transmission gate (pass gate), and plot it as a function of the output voltage. **07**

(b) Define and briefly discuss following: **07**

1. Yield
2. Positive photoresist
3. Substrate bias effect (body effect)
4. Noise margin
5. Master –slave flip-flop
6. Controllability in testing
7. PLD

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