Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE SEM-VIII Examination May 2012

Subject code: 180802

Subject Name: VLSI Technologies

Date:12/05/2012 **Time: 10.30 am – 01.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss VLSI design flow in brief.	**07**
	(b)	Explain Channel Length Modulation.	**04**
	(c)	Why is the size of PMOS transistor chosen to be 2.5 times of an NMOS transistor in CMOS Inverter?	**03**
Q.2	**(a)**	Explain any one down scaling techniques for MOSFET. Which technique is preferable?	**07**
	(b)	Design a resistive load inverter with R = 1kΩ, such that V_{OL} = 0.6V. The enhancement type nMOS driver transistor had following parameters: V_{DD} = 5 V, V_{TO} = 1 V, γ =0.2 $V^{1/2}$, λ = 0, $\mu_n.C_{OX}$ = 22.0 $\mu A/V^2$. Find the required aspect ratio W/L, V_{IL}, V_{IH} and Noise Margins NM_L and NM_H.	**07**
		OR	
	(b)	Draw the CMOS Inverter circuit and VTC for different operation regions of the nMOS and pMOS transistor. Derive the equation for threshold voltage of inverter.	**07**
Q.3	**(a)**	Derive the expression for drain current as a function of V_{GS}, V_{DS} and V_{SB} for all three region of operation of MOSFET using Gradual Channel Approximation.	**07**
	(b)	Explain fabrication process of nMOS transistor with diagram.	**07**
		OR	
Q.3	**(a)**	Discuss basic steps of the LOCOS Process.	**07**
	(b)	Draw & explain the basic structure of FPGA. Explain functioning of logic cell using lookup table approach.	**07**
Q.4	**(a)**	Discuss Complementary pass transistor logic. Realize the XOR gate using CPL.	**07**
	(b)	Explain Voltage Bootstrapping.	**07**
		OR	
Q.4	**(a)**	Explain the basic principle of Pass transistor circuits. Also Explain logic '1' transfer.	**07**
	(b)	Explain True Single Phase Clocking dynamic CMOS Logic.	**07**
Q.5	**(a)**	Discuss Built-in Self Test (BIST) Techniques.	**07**
	(b)	Discuss Controllability and Observability.	**07**
		OR	
Q.5	**(a)**	List the important concern for the IC packaging technology. Also Explain different packaging technologies.	**07**
	(b)	Give comparison between FPGA and CPLD.	**07**

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