Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI • EXAMINATION – SUMMER • 2014

Subject Code: 161004 Date: 28-05-2014

Subject Name: VLSI Technology and Design

Time: 10:30 am - 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1

(a) Explain the VLSI design flow using the D'Gajski's 'Y' – chart. **7**

(b) Explain the LOCOS technique for device isolation. Why it is preferred over the Etched field oxidation technique? **7**

Q.2

(a) Discuss the four components of threshold voltage (V_T) in detail. **7**

(b) Explain the Short Channel Effects on threshold voltage and mobility of the charge carriers. **7**

OR

(b) Calculate the threshold voltage V_{T0} at $V_{SB} = 0$, for a polysilicon gate *nMOS* transistor, with the following parameters: **7**

Substrate doping density $N_A = 3.5 \times 10^{16}\ cm^{-3}$

Polysilicon gate doping density $N_D = 4 \times 10^{20}\ cm^{-3}$

Gate oxide thickness $t_{ox} = 800\ A°$

Oxide-interface fixed charge density $N_{ox} = 6.5 \times 10^{10}\ cm^{-2}$.

Physical and material constants :

Thermal voltage $kT/q = 26\ mV$

Energy Gap of silicon(*Si*) $E_g = 1.12\ eV$

Intrinsic Carrier Concentration of (*Si*) $n_i = 1.45 \times 10^{10}\ cm^{-3}$

Dielectric constant of vaccum $\varepsilon_o = 8.85 \times 10^{-14}\ F/cm$

Dielectric constant of silicon $\varepsilon_{si} = 11.7 \times \varepsilon_o\ F/cm$

Dielectric constant of silicon dioxide $\varepsilon_{ox} = 3.97 \times \varepsilon_o\ F/cm$

Q.3

(a) Explain the MOSFET capacitances in detail. **7**

(b) Consider a CMOS inverter with the following parameters: **7**

nMOS $V_{T0,n} = 0.6\ V$, $\mu_n C_{ox} = 60\ \mu A/V^2$ $(W/L)_n = 8$

pMOS $V_{T0,p} = -0.7\ V$, $\mu_p C_{ox} = 25\ \mu A/V^2$ $(W/L)_p = 12$

Calculate the noise margins and the switching threshold (V_{th}) of this circuit.

The power supply voltage $V_{DD} = 3.3\ V$.

OR

Q.3

(a) Draw the inverter circuit with *depletion type nMOS* load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} and V_{IH} for depletion- load inverter. **7**

(b) Write a note on CMOS Ring Oscillator circuit. **7**

Q.4

(a) Define propagation delay and derive the expression for τ_{PHL} for CMOS Inverter. Assume ideal step as an input to CMOS Inverter. **7**

(b) Explain the basic principle of pass transistor circuit. Explain logic '1' transfer and logic '0' transfer. **7**

OR

Q.4

(a) Explain the dynamic CMOS logic (Precharge – Evaluation) and discuss the cascading problem in dynamic CMOS logic. **7**

(b) Explain the Transmission Gate (TG). Draw six-transistor CMOS -TG implementation of the XOR function. **7**

Q.5

(a) Explain Latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up. **7**

(b) Implement the following Boolean function using CMOS. **7**

$$F = \overline{(ABC + DE)}$$

Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that $(W/L)p = 20$ for all pMOS transistors and $(W/L)n = 10$ for all nMOS transistors.

OR

Q.5 Write short note (Any TWO) **14**

(a) On-Chip Clock Generation and Distribution.

(b) Comparison of FPGA and CPLD.

(c) Comparison of Full-scaling and Constant voltage scaling.

(d) Built In Self Test (BIST).

(e) Domino CMOS logic.

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