Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII • EXAMINATION – SUMMER • 2014

Subject Code: 170907 Date: 31-05-2014

Subject Name: Advanced Microcontrollers and Embedded Systems

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain SPI communication protocol for 8051 microcontroller.	**07**
	(b)	What is PLL? Explain how it is used for generating the required system clock frequency in CIP-51Microcontrollers.	**07**
Q.2	**(a)**	Draw and explain architecture of CIP-51 family.	**07**
	(b)	Discuss I^2C communication protocol for 8051 microcontroller.	**07**
		OR	
	(b)	Explain the PCA Timer interrupt structure and Edge-triggered mode of C8051F120 with block diagram.	**07**
Q.3	**(a)**	Enlist advanced features of CIP51 as compare to normal 8051	**07**
	(b)	Discuss use of Watch-dog timer for embedded systems?	**07**
		OR	
Q.3	**(a)**	Explain the round robin with interrupt architecture.	**07**
	(b)	Explain functional queue scheduling architecture.	**07**
Q.4	**(a)**	Discuss the interfacing of 89C51 controller to RTC.	**07**
	(b)	Draw & explain interfacing of DAC with 8051.	**07**
		OR	
Q.4	**(a)**	What is Scheduler in RTOS? Explain Task and Task States in detail with suitable diagram.	**07**
	(b)	What is SFR Paging? Why SFR Paging is required in CIP51 Controllers?	**07**
Q.5	**(a)**	Explain the operation of UART & communication with PC.	**07**
	(b)	Draw & explain interfacing of E^2PROM with 8051.	**07**
		OR	
Q.5	**(a)**	Discuss programming of general purpose I/Os of CIP-51 microcontroller.	**07**
	(b)	Explain semaphores & shared data in Real Time Operating System.	**07**

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