Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII • EXAMINATION – SUMMER 2014

Subject Code: 171701 **Date: 22-05-2014**

Subject Name: *Control System Design*

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Give the complete design process of lead compensator in frequency domain. **07**

(b) Explain controllability, observability and duality for the both of them. **07**

Q.2 **(a)** Verify the controllability of the system described as follows. **07**

$\dot{x}_1 = x_2 + u_1$

$\dot{x}_2 = x_3$

$\dot{x}_3 = -2x_2 - 3x_3 + u_1 + u_2$

(b) For given transfer function of control system , verify the observability. **07**

$$\frac{Y(s)}{U(s)} = \frac{s+2}{S^3+9s^2+26s+24}.$$

OR

(b) Explain the optimal control for full state feedback control system. **07**

Q.3 **(a)** Discuss the robust control system with uncertain parameters. **07**

(b) Discuss the robust internal model system. **07**

OR

Q.3 **(a)** Determine the z-transform and sketch the ROC of **07**

$$x(n) = \{a^n \cos\omega_0 n\}u(n)$$

(b) Obtain Z-inverse of the following for ROC $z > 1$ and $z < 0.5$. **07**

$$X(Z) = \frac{1+Z^{-1}}{1-Z^{-1}+0.5Z^{-2}}.$$

Q.4 **(a)** Give the design for dead beat response. **07**

(b) Discuss the design of robust PID control system. **07**

OR

Q.4 **(a)** Explain closed loop system with digital computer compensation. **07**

(b) Give the realization of sampled data system for digital control. **07**

Q.5 Design a lag compensator for a system G(s) to meet following specification. **14**

$G(s) = \frac{K}{s(s+1)(s+4)}$ use frequency domain analysis.

Damping ratio =0.4, settling time = 10 second, velocity error constant $\geq 5\ sec^{-1}$

OR

Q.5 Design suitable compensator for a system G(s) to meet following specification. **14**

$G(s) = \frac{K}{s^2}$ use time domain analysis.

settling time ≤ 4 second, peak over shoot for step input $\leq 20\%$

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