Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII • EXAMINATION – SUMMER 2014

Subject Code: 180908 Date: 27-05-2014

Subject Name: Advanced Processor and Controller

Time: 10:30 am TO 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	State and explain in short the components of C2xx core of TMS320LF2407 DSP from Texas Instrument.	**07**
	(b)	Sketch and explain the hardware components of PLC.	**07**
Q.2	**(a)**	(i)Describe features of ADC available in TMS320LF2407 DSP.	**04**
		(ii) Describe the important properties of LTI system.	**03**
	(b)	Sketch and explain interrupt structure of LF2407 DSP.	**07**
		OR	
	(b)	(i) Describe in short the various discrete systems.	**04**
		(ii) How Ex-OR, NAND and NOR logic is realized on a ladder diagram?	**03**
Q.3	**(a)**	Sketch and explain Program Memory map of LF2407 DSP.	**07**
	(b)	Draw the ladder diagram for traffic light sequence using time delay on timers. At momentary start only RED lamp should be ON for 60 Sec, than RED and YELLOW lamp should be ON for 10 Sec, followed by only GREEN should be ON for 60 Sec. then YELLOW lamp ON for 10 Sec. and the sequence repeats.	**07**
		OR	
Q.3	**(a)**	Sketch and explain Data Memory map of LF2407 DSP.	**07**
	(b)	Compute and plot convolution of two signals using tabulation method. $h(n) = \{1, 2, 1, -1\}$ and $x(n) = \{1, 2, 3, 1\}$	**07**
Q.4	**(a)**	Explain the Addressing modes used by C2xx core Instruction set of LF2407 giving examples.	**07**
	(b)	Describe the properties of Z- Transform.	**07**
		OR	
Q.4	**(a)**	Explain the general I/O pins functionality using its associated registers.	**07**
	(b)	Determine the Z-Transform and plot ROC for the sequence $x(n) = (-1/8)^n u(n) - (1/4)^n u(-n-1)$	**07**
Q.5	**(a)**	Explain in brief the sub-components of Event Manager module in LF2407 DSP.	**07**
	(b)	(i) Describe the major external registers used by PLC.	**03**
		(ii)Describe two analog modules used by PLC.	**04**
		OR	
Q.5	**(a)**	Write sequential steps to generate 50% duty cycle PWM using general purpose timer compare function. Also write ALP for the same with PLL set to CLKIN x 4, WD disable and wait state generator set for zero wait state.	**07**
	(b)	(i) Describe PLC counter functions.	**04**
		(ii)Describe the bit function used by PLC.	**03**

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