Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII • EXAMINATION – SUMMER 2013

Subject Code: 180802 Date: 13/05/2013

Subject Name: VLSI Technologies

Time: 10:30 am TO 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain different criteria to be considered to measure the design quality. **07**

(b) Discuss basic steps of Fabrication process flow. **07**

Q.2 **(a)** Explain two technology scaling methods, namely (i) constant field scaling and (ii) constant supply voltage scaling. In particular for both the cases, show analytically by using equations how the doping densities, power dissipation and power density are affected in term of the scaling factor, S. **07**

(b) Explain basic steps of LOCOS process. What is birdôs beak region? **07**

OR

(b) Explain major types of MOSFET capacitances and show its variations under different operating conditions and physical parameters. **07**

Q.3 **(a)** Explain the functioning of depletion type NMOS inverter and derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH} for the same. **07**

(b) Derive the equation of threshold voltage for CMOS Inverter circuit. Also prove that for symmetric CMOS $(W/L)_p = 2.5\ (W/L)_n$. **07**

OR

Q.3 **(a)** Explain different physical parameters affecting the threshold voltage of MOS structure. **07**

(b) Consider a CMOS inverter circuit with the following parameters: **07**
VDD = 3.3 V, $V_{TO,n}$ = 0.6 V, $V_{TO,p}$ = ï 0.7 V,
$k_n = 200\ \mu A/V^2$, $k_p = 80\ \mu A/V^2$.
Calculate the noise margin of the circuit.

Q.4 **(a)** Derive the expression for Ű$_{PHL}$. Draw input and output waveform during high to low transition of output for CMOS Inverter. **07**

(b) Implement following Boolean functions using CMOS Transmission Gate(TG): **07**
(i) F1 = AB + AðCô + ABðC
(ii) F2 = AB + AðBô

OR

Q.4 **(a)** Explain CMOS Transmission Gate in detail. **07**

(b) Explain CMOS D ï Latch and edge triggered Flip-Flop. **07**

Q.5 **(a)** Discuss NORA CMOS Logic. **07**

(b) Discuss Scan Based Techniques for Testing. **07**

OR

Q.5 **(a)** Explain Voltage Bootstrapping. **07**

(b) Describe different Ad HOC testable design techniques. **07**

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