Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: 2132003 Date: 20-12-2014

Subject Name: Design Concepts in Basic Electronics

Time: 02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following question. **07**

(1) Define Digital Signal.

(2) Convert $(145)_{10}$ into its equivalent Binary.

(3) Convert $(100101010110)_{2}$ into its equivalent Octal and Hexadecimal number.

(4) Convert $(1F67.546)_{16}$ into its equivalent Decimal.

(5) Convert $(6)_{10}$ in to equivalent BCD, Gray code and Excess-3 code.

(6) State the truth table of Full-Adder.

(7) State excitation table and characteristics table for J K Flip Flop.

(b) Prove the following using Truth Table. **07**

(1) $$\bar{A} + \bar{B} + \bar{C} = \overline{(A \cdot B \cdot C)}$$

(2) $$XY + \bar{X}Z + YZ = XY + \bar{X}Z$$

Q.2 **(a)** Explain in detail different type of breakdown in diode. **07**

(b) Simplify the following Boolean function using Karnaugh map method and realize with minimum NAND gates only. **07**

Function F (A,B,C,D) = ∑ (0,1,2,8,9) and

don't care conditions: d(A,B,C,D) = ∑ (3, 5,10,13)

OR

(b) Reduce following Boolean expression in minimum number of literals. **(ANY TWO)** **07**

(1) $$AB + A(B + C) + B(B + C)$$

(2) $$\bar{X}YZ + XZ + \bar{X}Z$$

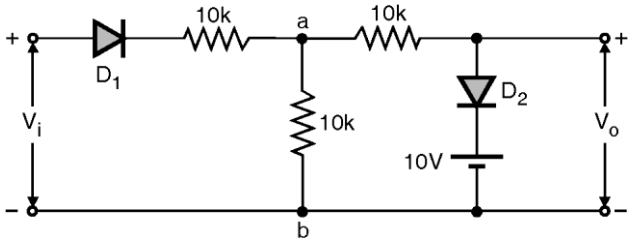
Q.3 **(a)** Design 3 bit up – down synchronous counter with help of T flip flop. **07**

(b) Give the points of difference between half wave, Full wave, and Bridge rectifier. **07**

OR

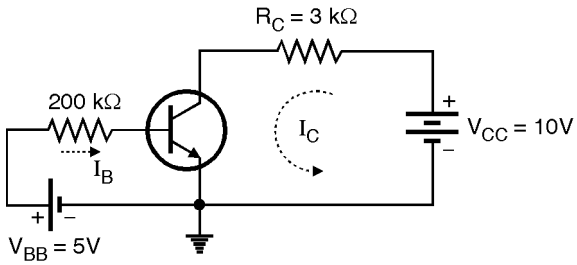
Q.3 **(a)** Show that NAND and NOR are universal gate. **07**

(b) The diodes are ideal, plot Vo against Vi indicating all intercepts, slopes and voltage levels for Fig. and Sketch Vo if Vi = 40 sin ωt. **07**



Q.4 **(a)** Explain with neat diagram working of 8x1 multiplexer and 3to8 decoder. **07**

(b) For the transistor shown in Fig, β = 100. Find the transistor currents and state in which region it is operating. Assume that it is a silicon transistor **07**



OR

Q.4 **(a)** Explain with neat diagram working of 4-bit bidirectional shift register with parallel load **07**

(b) Explain in details effect of temperature, transistor and collector current on β_{dc} **07**

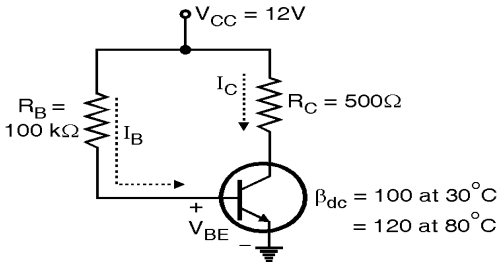
Q.5 **(a)** Explain the input output characteristic of n-p-n transistor in CE configuration. Also indicate different regions. **07**

(b) Explain with neat diagram Voltage divider bias **07**

OR

Q.5 **(a)** Explain the input output characteristic of n-p-n transistor in CB configuration. Also indicate different regions. **07**

(b) The fixed bias circuit of Fig. a silicon transistor is uses. The component values are R_C = 500 Ω and R_B = 100 kΩ. β_{dc} of the transistor is 100 at 30°C. Determine Q point co-ordinates at 30°C. **07**



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