

GUJARAT TECHNOLOGICAL UNIVERSITY
B. E. - SEMESTER – III • EXAMINATION – WINTER 2012

Subject code: 130701**Date: 04-01-2013****Subject Name: Digital Logic Design****Time: 10.30 am – 01.00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** Convert the decimal number 250.5 to base 3, base 4, base 7, base 8 and base 16 **14**
- Q.2** (a) Show how a full-adder can be converted to a full-subtractor with the addition of one inverter circuit. **07**
 (b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit. **07**
- OR**
- (b) Construct 4x16 decoder with two 3x8 decoders. **07**
- Q.3** (a) Find the complement of the following Boolean function and reduce to a minimum number of literals. **07**
 $B'D + A'BC' + ACD + A'BC$
 (b) Obtain the simplified expressions in sum of products using K-map: $x'z + w'xy' + w(x'y + xy')$ **07**
- OR**
- Q.3** (a) Simplify the following Boolean function by means of the tabulation method: **07**
 $F(A,B,C,D,E,F,G) = (20,28,38,39,52,60,102,103,127)$
 (b) Explain JK Flipflop. What is the disadvantage of it and how it can be eliminated? **07**
- Q.4** (a) Design a counter with the following binary sequence: **07**
 0, 1, 3, 7, 6, 4 and repeat. Use T flipflop.
 (b) Explain BCD Ripple counter and draw its logic diagram and timing diagram. **07**
- OR**
- Q.4** (a) Explain in detail bidirectional shift register with parallel load. **07**
Q.4 (b) Explain PLA with necessary diagrams. **07**
- Q.5** Explain arithmetic, logic and shift microoperations in detail. **14**
- OR**
- Q.5** (a) Explain bus organization for four processor register and ALU connected through common buses. **07**
 (b) Distinguish between microprogram control and hard-wired control. **07**
