Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

B. E. - SEMESTER – III • EXAMINATION – WINTER 2012

Subject code: 130902 Date: 04-01-2013

Subject Name: Analog and Digital Electronics

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the equivalent circuit with significance of each component of a practical OP-AMP.	**07**
	(b)	List and Discuss all ideal characteristics of an Op Amp.	**07**
Q.2	**(a)**	Explain voltage follower and inverter using Op- Amp.	**07**
	(b)	Draw functional block diagram of IC 555 & discuss function of each pin.	**07**
		OR	
	(b)	Explain integrator with its frequency response.	**07**
Q.3	**(a)**	Explain the Universal Gate and build up AND, OR and NOT using NAND and NOR gate.	**07**
	(b)	Derive Full Adder with the help of necessary truth table, K- Map. Also express in AOI logic diagram.	**07**
		OR	
Q.3	**(a)**	Derive Full Subtractor with the help of necessary truth table, K- Map. Also express in AOI logic diagram.	**07**
	(b)	Do as directed 1) $(3F8)16 + (5B3)_{16} = (\quad)_{16}$ 2) $(231.23)_4 = (\quad)_{10}$ 3) $(111101100)_2 = (\quad)_8$	**07**
Q.4	**(a)**	Define the following general characteristics of logic families. (i) Propagation Delay (ii) Noise Margin (iii) Fan-in (iv) SOP (v) POS(vi)Fan-Out (vii) Power Dissipation	**07**
	(b)	1) Subtract with unsigned binary no using 2's complement of subtrahend :x=1010100, y=1000011 , perform x-y 2) Subtract with unsigned binary no using 10's complement of subtrahend x=3250, y=72532 , perform x-y.	**07**
		OR	
Q.4	**(a)**	Simplify the following 1) xy + xyz + xyz' + x'yz 2) x + x'y+ xy'	**07**
Q.4	**(b)**	Give classification of registers. Discuss 4 – bit buffer register using D – flip flop	**07**
Q.5	**(a)**	i) Minimize the following Boolean expression using K-map. $Y = \Sigma m(0,1,4,8,9,10)$ ii) Discuss multiplexers with suitable diagram	**07**
	(b)	Explain the working of Master-Slave J-K flip-flop	**07**
		OR	
Q.5	**(a)**	Define decoders, encoder and de-multiplexer Give application of each	**07**
	(b)	State and explain the triggering methods for a T- flip flop.	**07**

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