Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

B. E. - SEMESTER – III • EXAMINATION – WINTER 2012

Subject code: 131101 Date: 07-01-2013

Subject Name: Basic Electronics

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain followings: **07**

(i) Electron volt.
(ii) Mobility
(iii) Barrier potential
(iv) Diffusion current
(v) Mean life time of a carrier
(vi) Graded semiconductor
(vii) Intrinsic concentration

(b) Explain Hall effect with neat sketch. Discuss how to measure charge density and mobility for a given specimen of semiconductor using Hall Effect? **07**

Q.2 **(a)** Specimen of material is 5 cm long and having radius of 5 mm. Current is due to electrons whose mobility is 5000 cm^2/V.s. Current of 50 mA flows through it when 0.5 Volt is impressed across it. Calculate concentration of free electrons and drift velocity. **07**

(b) Explain potential variation in graded semiconductor. **07**

OR

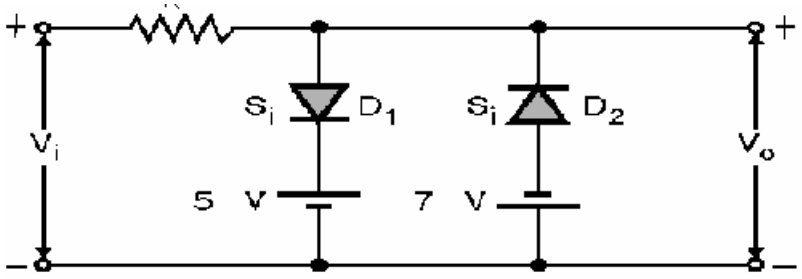
(b) Derive the flowing equation for current density. **07**

$J = nq\mu\varepsilon$

Q.3 **(a)** (i) Describe two breakdown mechanisms in a p-n junction diode. **04**

(ii) Why the name varicap is given to varactor diode? Give its two applications. **03**

(b) A sinusoidal voltage peak value of 10V and frequency 50 Hz is applied at the input of clipping circuit shown in figure below. Draw output voltage waveform and transfer characteristic. Assume both diodes are ideal. **07**



OR

Q.3 **(a)** (i) Draw symbol of tunnel diode, Draw VI characteristic of tunnel diode and explain it. **04**

(ii) Explain how Zener diode regulates voltage. **03**

(b) A sinusoidal voltage peak value of 40V and frequency 50 Hz is applied at the input of a half wave rectifier, No filter is used. The Load resistance is 500 Ω. Neglect cut-in voltage. Diode has $R_f = 5\ \Omega$ and $Rr = \infty$. **07**

(i) Draw Output voltage waveform and derive expression for DC output voltage.

(ii) Calculate DC value of load current, rms value of load current and Rectification efficiency.

Q.4 **(a)** (i) Derive relation between α and ß for a transistor. **04**

(ii) Why CE configuration is preferred for amplification? **03**

(b) Draw a fixed bias circuit. State advantages and disadvantages of fixed bias circuit. Specify components value to have operating point at (9V, 2mA). Take VCC = 12 V and ß = 70. **07**

OR

Q.4 **(a)** (i) In npn transistor α = 0.98, I_E = 20 mA, I_{CBO} = 3μA. Determine I_C, I_B, ß and I_{CEO} **04**

(ii) What is early effect in CB configuration? Explain with graph. **03**

Q.4 **(b)** Draw collector to base bias circuit and explain its operation. Also state advantages and disadvantages of the circuit. **07**

Q.5 **(a)** Draw Emitter follower circuit. Obtain Hybrid equivalent circuit and derive expression for current gain. **07**

(b) (i) Does thermal runaway take place in FET? Why? **03**

(ii) Define parameters of FET and state relationship among them. **04**

OR

Q.5 **(a)** Determine Av, Ai, Ri and Ro for a common emitter amplifier using a transistor with hie = 1200 Ω, hfe = 36, hre = 0 and hoe = 2×10^{-6} mho. Use RL = 2.5 K Ω, RS = 500 Ω and neglect the effect of biasing circuit. **07**

(b) (i) Explain in what respect a power amplifier differ from a voltage amplifier? **03**

(ii) Prove that the maximum theoretical collector circuit efficiency of a class A amplifier is 50% **04**

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