Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: 2130306 Date:30/12/ 2014

Subject Name: Fundamentals of Digital Design

Time:02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain half and full adders in detail.	**07**
	(b)	Implement the functions F=∑(0,3,4,6,8,10,12,14) with don't care conditions d=∑(1,2,9,11) Discuss the effect of don't care conditions.	**07**
Q.2	**(a)**	Convert the following numbers as directed: 1. $(13.23)_{10} = (\ )_2$ 2. $(10110.11)_2 = (\ )_{10}$ 3. $(110111011101.111011)_2 = (\ )_8$	**07**
	(b)	What is Multiplexer? With logic circuit and function table explain the working of 4 to 1 line multiplexer.	**07**
		OR	
	(b)	Simplify the Boolean Function by using the tabulation method: F = Σ(0,1,2,8,10,11,14,15)	**07**
Q.3	**(a)**	Simplify the following Boolean functions to a minimum numbers of literals. (a) xyz+x'y+xyz' and (b)(A+B)'(A'+B')'	**07**
	(b)	Perform the subtraction with the following decimal numbers using 1's compliment and 2's compliments. (a) 1100-1101 , (b) 1010-1000	**07**
		OR	
Q.3	**(a)**	Show that the dual of the exclusive-OR is equal to its compliment.	**07**
	(b)	Obtain the simplified expression for the following Boolean functions using K-MAP method. 1. F(A,B,C,D) = ∑(0,1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15) 2. F(A,B,C,D) =∑(11,12,13,14,15).	**07**
Q.4	**(a)**	Design Sequential Circuit with J.K. Flip Flops to satisfy the following state equation. 1. A(t + 1) =A'B'CD + A'B'C + ACD +AC'D' 2. B(t+1)= A'C + CD'+ A'BC' 3. C(t + 1) = B 4. D(t +1)=D'	**07**
	(b)	Design and implement BCD to GRAY code converter.	**07**
		OR	
Q.4	**(a)**	Explain 4 bit Magnitude Comparator.	**07**
	(b)	Give the difference between Combinational and sequential circuits and also explain state diagram machine.	**07**
Q.5	**(a)**	What is the full form of FPGA? Explain the basic block diagram of FPGA.	**07**
	(b)	Explain Master slave flip-flop in detail.	**07**
		OR	
Q.5	**(a)**	Explain D type positive edge triggered flip flop.	**07**
	(b)	What is encoder? Explain the working of Octal to binary Encoder.	**07**

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