Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 3715501 **Date: 06-01-2015**

Subject Name: Advanced Computer Architecture

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What are the CPU ï GPU Synchronization issues	**07**
	(b)	Explain 3 stage pipeline in ARM architecture	**07**
Q.2	**(a)**	Explain Data Hazard in detail.	**07**
	(b)	Explain the below mentioned concepts and differentiate them. 1.RISC and CISC 2. Big-endian and Little-endian.	**07**
		OR	
	(b)	Explain cache coherency in detail?	**07**
Q.3	**(a)**	Describe in brief Interrupt Controller MPCore processors	**07**
	(b)	Explain SIMD instructions in brief	**07**
		OR	
Q.3	**(a)**	Draw block diagram of Unified instruction and data cache	**07**
	(b)	What is Snoop control unit (SCU).	**07**
Q.4	**(a)**	Draw block diagram of Harvard architecture based data and instruction caches	**07**
	(b)	List down 3 major Bus Transactions and explain	**07**
		OR	
Q.4	**(a)**	Explain about Translation Look-Aside Buffer	**07**
	(b)	Describe a typical Typical TLB Format	**07**
Q.5	**(a)**	Explain memory Segmentation (related to MMU) in brief	**07**
	(b)	Explain Paging memory management ?How Paging related to MMU	**07**
		OR	
Q.5	**(a)**	Explain about Basic VLIW Design Principles? What are Implications for Compilers design in VLIW.	**07**
	(b)	What is a toolchain. What are essential components of a toolchain and explain each.	**07**

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