Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

Diploma Engineering - SEMESTER–III • EXAMINATION – SUMMER • 2014

Subject Code: 3331703 Date: 17-06-2014

Subject Name: Digital Techniques

Time: 10:30 am - 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Each question carry equal marks (14 marks)**

Q.1 (a) Convert the following numbers to Decimal.(Any Two) **07**

1. $(1001001.011)_2$ 2. $(367.12)_8$ 3. $(AFC56.DE)_{16}$

(b) Convert the following numbers .(Any Two) **07**

1. $(100111001.0111)_2$ to (_____)$_8$
2. $(514.15)_8$ to (_____)$_{16}$
3. $(597.125)_{10}$ to (_____)$_2$

Q.2 (a) Perform the subtraction using 1's Complement. Check the answer by straight subtraction. (Any Two) **07**

1. 11010 – 1101 2. 10010 – 10011 3. 11010 – 10000

(b) Perform the subtraction using 2's Complement. Check the answer by straight subtraction. (Any Two) **07**

1. 11110 – 11010 2. 10110 – 10011 3. 11111 – 10001

OR

(b) Perform the following binary operations. (Any Two) **07**

1. $(11110110)_2$ X $(11011011)_2$
2. $(1101101)_2$ / $(1100)_2$
3. 11111+ 10001+11011-11010 = (_____)$_2$

Q.3 (a) Prove the following. (Any Two) **07**

1. X + X'Y = X + Y 2. X (X' + Y) = XY
3. Simplify the following expression in SOP form. F(a,b,c) = ∑(2,3,6,7)

(b) State and prove D' Morgan's theorem. **07**

OR

Q.3 (a) Draw AND, OR, and EX-OR gates using NOR as a universal gate. **07**

(b) Simplify the following expression in SOP form using Karnaugh Map. **07**
F(a,b,c,d) = ∑(2,3,12,13,14,15)

Q.4 (a) Draw the logic diagram of FULL_ADDER using two HALF_ADDER and OR gate. **07**

(b) What is the importance of multiplexer? Draw and Explain logic diagram of 4 to1 line multiplexer. **07**

OR

Q. 4 (a) Draw the logic diagram of 4-bit Binary to gray code converter. **07**

(b) Draw the logic diagram of 3 to 8line Decoder. **07**

Q.5 (a) Draw and explain 4 bit ripple counter. **07**

(b) With logic circuit and truth table explain J-K flip flop. **07**

OR

Q.5 (a) Design logic circuit using logic gates for pressure logic operation having pressure switch configuration HH, LL. **07**

(b) Design logic circuit using gates for flow logic operation having flow switch HH, H ,L ,LL. **07**

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