Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

MCA. Sem- IST Regular / Remedial Examination January-February 2011

Subject code: 610004

Subject Name: Fundamentals of Computer Organization

Date:01 /02 /2011 **Time: 10.30 am – 01.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as directed: **01**

i. $(110111.1)_2 / (101)_2 = (\ \_\_\_\_\_\ )_2$.

ii. $(BC70.0E)_{16} = (\ \_\_\_\_\_\ )_8$. **01**

iii. 46 – 84 = _____. **01**
(Use 12-bit 1's Complement method)

iv. $(1101101101101.101101)_2 = (\ \_\_\_\_\_\ )_{16}$. **01**

v. Convert binary number 110110110 to its equivalent grey code. **01**

vi. Convert grey code 100011101 to its equivalent binary number. **01**

Vii For the given message code 1110111, detect & correct using 7-bit even-parity hamming code. **01**

(b) Do as directed: **01**

i. Convert 4228.5 to its equivalent 8421 BCD code.

ii. Convert given binary number 011101110111.0111 to its equivalent XS-3 code. **01**

iii. Simplify the given Boolean expression: AB′C + A′BC + ABC **01**

iv. De Morganize the given Boolean expression: [((A+B) ′.(C+D) ′)′.((E+F)′.(G+H)′)′]′ **01**

v. Draw the block diagram of digital computer. State the purpose of each component. **03**

Q.2 **(a)** Explain Memory Address Map. **07**

(b) List various types of printers and explain any one of them. **07**

OR

(b) Explain Visual Display Unit. **07**

Q.3 **(a)** Design and explain Full adder circuit. **07**

(b) i. Which registers are available in DMA controller? State their purpose. **04**

ii. Why read and write are control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs? **03**

OR

Q.3 **(a)** Design and explain BCD adder. **07**

(b) Explain Handshaking method of Asynchronous Data Transfer. **07**

Q.4 **(a)** Write a program to evaluate arithmetic statement: **07**
X = ((A*B) + (C*D-E)) / (A+B)
- using general register computer with three address instruction format and accumulator type computer with one address instruction format

(b) Construct a 3 × 8 decoder using two 2 × 4 decoder. **07**

OR

Q.4 **(a)** An instruction is stored at location 300 with its address field at location 301, the address field has the value 400. A processor register R1 contains value 200. Evaluate effective address if addressing mode of instruction is : (a) direct (b) immediate (c) relative (d) register indirect (e) index with R1 as index register. **07**

(b) Explain the design of 8-to-1 line Data Selector. **07**

Q.5 **(a)** i. Draw a set of waveforms for S & R and X & X′ so that Flip-flop will have output signals 0011010 on output line. **04**

ii. Draw and explain 4-bit shift right register. **03**

(b) Do as directed: **01**

i. Reduce using K-map: ∑m(5,6,7,9,10,11,13,14,15).

ii. Reduce using K-map: ∑m(9,10,12)+d(3,5,6,7,11,13,14,15) **01**

iii. Write the dual of given Boolean expression: **01**
AB + (AC) ′ + AB′C(AB+C) = 1

iv. Write any one form Absorption law and prove by the method of perfect induction. **02**

v. Derive a Boolean expression (in SOP form) for a logic circuit that will have a 1 output when X=0, Y=0, Z=1 and X=1, Y=1, Z=0 and a 0 output for all other input states. **02**

OR

Q.5 **(a)** i. Design a 2-bit up counter which goes through states 00,01,10,11 and 00 and so on when external input is 1 and state remains unchanged when external input is 0. **04**

ii. Explain Master-Slave Flip-flop. **03**

(b) i. What do you mean by universal gate? Which gates are universal gates? Why ? **05**

ii. Derive a Boolean expression (in POS form) for a 3-input gating network that will have outputs 0 when all the 3-inputs are same. The outputs are to be 1 for all other cases. **02**

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