

GUJARAT TECHNOLOGICAL UNIVERSITY**MCA - SEMESTER-I • EXAMINATION – WINTER 2013****Subject Code: 2610004****Date: 24-12-2013****Subject Name: Fundamentals of Computer Organization****Time: 02:30 pm TO 05:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** Define the following in one or two lines: **07**
- i. Radix.
 - ii. Gate
 - iii. Flip-flop
 - iv. Subcube
 - v. Accumulator
 - vi. Product Term
 - vii. Code Segment(CS)
- (b)**
- i. Convert the Decimal number into Binary and Octal: 2048.0625 **02**
 - ii. State the commutative and associative laws of Boolean algebra. **02**
 - iii. What is Binary Half-Adder? Give its design diagram and truth table. **03**

- Q.2 (a)** Explain the basic components of a Digital Computer with the Block Diagram of Typical Digital Computer. **07**
- (b)** Draw the NAND gate network, AND-to-OR gate network for the output: **07**
 $AB + CD + EF$

OR

- (b)** Using K-map simplify the following expressions in four variables, W, X, Y, and Z: First specify the terms in Product terms and then construct the map for simplification. **07**

$$m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$$

- Q.3 (a)** Write notes on Shift Register with its block diagram and wave diagram. **07**
- (b)** Consider the following three-input-variable table and derive SOP and POS expressions and then simplify them. **07**

INPUTS			OUTPUT
X	Y	Z	A
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

OR

- Q.3 (a)** Explain the operations of a Binary Counter with its block diagram and wave diagram. **07**
- (b)** Explain the process of addition using 1's and 2's complement system. **07**

- Q.4 (a)** How to make a BCD adder by using full-adders and AND and OR gates? **07**
Explain with one example.
- (b)** Construct a Multiplexer that selects one input from available 8 inputs. **07**
Explain with a block diagram.

OR

- Q.4 (a)** Design a decoder which is completely parallel to decode three flip-flops. **07**
Explain with its block diagram.
- (b)** Write notes on Dynamic Random-Access Memories with necessary **07**
diagrams.

- Q.5 (a)** Explain the three different sections of bus. Draw the timing of **07**
synchronous data transfers involving the sections.
- (b)** What are the different techniques used in giving memory address to an **07**
instruction? Explain any two with examples.

OR

- Q.5 (a)** Draw the block diagram of 8086 Microprocessor. Explain its Bus **07**
Interfacing Unit.
- (b)** Explain the general format of Instructions of 8086. Give the template for **07**
MOV Instruction.
