Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-II Examination July 2010

Subject code: 710412

Subject Name: Digital VLSI Design

Date: 08 / 07 /2010 **Time: 11.00am – 1.30pm**

Total Marks: 60

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Draw necessary neat sketch wherever necessary.**

Q.1 **(a)** What do you mean by MOSFET Scaling ? Explain Constant-field Scaling and Constant-voltage Scaling in detail. **06**

(b) Define τ_{PHL} and τ_{PLH} for CMOS inverter. Derive τ_{PHL} for CMOS inverter. **06**

Q.2 **(a)** Draw the VLSI design flow in terms of Y-chart. Discuss the each three domain of Y-chart in detail. **06**

(b) What is LOCOS technique ? Why it is required ? Explain LOCOS with neat sketches. **06**

OR

(b) Explain following process for VLSI fabrication with figures. (i) Oxidation (ii) Photolithography. **06**

Q.3 **(a)** Describe Accumulation, Depletion and Inversion process for the MOS system under external bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion. **06**

(b) What is Layout Design Rules ? Explain. Draw a neat sketch which shows the design rules which determines the dimension of a minimum size transistor. **06**

OR

Q.3 **(a)** Derive the equation of Drain current (I_D) for an N-channel MOSFET operating in a linear region. Draw the necessary sketch. **06**

(b) Write a detail note on Oxide related MOSFET Capacitances. **06**

Q.4 **(a)** Derive the switching threshold (V_{th}) for CMOS inverter. Also prove that for symmetric inverter $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$. **06**

(b) What is Euler path approach. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), $X = \overline{A(D+E)+BC}$. Explain the importance of Euler path approach. **06**

OR

Q.4 **(a)** Consider the CMOS inverter with following parameters. **06**

$V_{DD} = 3.5$ V , $k_n = 220\ \mu A/V^2$, $k_p = 85\ \mu A/V^2$,
$V_{TO,n} = 0.7$ V , $V_{TO,p} = -0.7$ V.
Calculate the noise margins of the circuit.

(b) Write a short note on CMOS Transmission Gate. Explain its usefulness. **06**

Q.5 **(a)** Explain the charge sharing problem in DOMINO CMOS logic. How it can be over come ? Suggest simple solution. **06**

(b) What is clock skew problem for NP-Domino CMOS Logic circuits. Explain True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits. **06**

OR

Q.5 **(a)** Explain the basic principle of pass transistor, using Logic "1" transfer event. How it is important in dynamic logic circuits. **06**

(b) Write a short note on Pre-discharge and Evaluate logic for dynamic logic circuits. **06**

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