Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. Sem. – II[nd] - Examination – June/July- 2011

Subject code: 1722602

Subject Name: CMOS Circuit Design II

Date:24/06/2011 **Time: 10:30 am – 01:00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** How can we achieve temperature-independent output voltage in voltage reference circuit? Explain the principle of operation in detail with necessary derivation. Show that if one voltage source is taken as V_{BE}, then second voltage source should be 17.2 V_T. **07**

(b) Show that the basic charge pump PLL behaves as low-pass filter for the jitter appearing in input signal and it behaves as high-pass filter for the jitter appearing in VCO signal. **07**

Q.2 **(a)** **1.** Suppose a type I (simple) PLL experiences a frequency step $\Delta\omega$ at $t = 0$. Calculate the change in phase error using Laplace transform. **07**

2. In type I PLL, an external voltage V_{ex} is added to the output of low-pass filter. (a) Determine the phase error and V_{LPF} if the loop is locked and $V_{ex} = V_1$. (b) Suppose V_{ex} steps from V_1 to V_2 at $t = t_1$. How the PLL will respond?

(b) Determine the small-signal output impedance of the bandgap reference circuit shown in Fig. Q:2 (b) and examine its behavior with frequency. **07**

OR

(b) In SC non-inverting amplifier (see Fig. Q:2 (b) OR), S_1 turns off Δt seconds after S_2 turns off, and S_3 turns on Δt seconds after S_1 turns off. Plot the output waveform taking into the charge injection and clock feedthrough of all switches. Assume all switches are implemented with NMOS. **07**

Q.3 **(a)** Show that the charge injection in NMOS/PMOS switch results into non-unity gain. dc offset, and non-linearity in V_{out} as a function of V_{in}. Explain the trade-off between charge injection and speed of the switch. **07**

(b) Explain the mechanism of erasing and writing data into flash memory. Draw circuit diagram for a 4-bit NAND flash memory cell and provide the table indicating levels of input signals for erase, program, and read operations. **07**

OR

Q.3 **(a)** How can we realize resistor using combination of switches and capacitor? Explain working of basic SC integrator circuit (with two switches), discuss the problems associated with its accuracy and draw SC integrator circuit which solves problem of basic SC integrator circuit. **07**

(b) Derive expression for final voltage on bit line capacitance when access transistor gets ON in one-transistor-one-capacitor (1T1C) **07**

DRAM. Assume that bit line capacitance is initially charged to $V_{DD}/2$.

Calculate the change in the voltage across bit-line capacitance (100 fF) for a V_{DD} = 1V and DRAM capacitor 20 fF. Assume that the logic one is stored in DRAM cell.

Q.4 **(a)** Draw and explain the block diagram of voltage comparator. Discuss the operation of positive feedback decision circuit with necessary equations in detail. **07**

(b) Explain the basic concept of using DSM (delta-sigma modulation) in sensing a flash memory. **07**

OR

Q.4 **(a)** What are the different performance parameters of voltage comparator? Explain in brief how would you measure each of them with diagrams and waveforms? **07**

(b) Explain the basic charge pump concept to generate positive voltage greater than V_{DD}. **07**

Q.5 **(a)** Explain the principle of chopper stabilization used to reduce effects of 1/*f* noise and input-offset voltage. Also explain that how it can be included in CMOS op-amp. **07**

(b) Define following terms related to DAC: 1. Dynamic range, 2. Quantization noise, 3. Signal-to-noise (SNR) ratio, and 4. Offset error. Derive expression for maximum value of SNR. **07**

OR

Q.5 **(a)** Draw commonly used differential input stage and derive expression for minimum value of V_{DD} such that all transistors are ON and operating in saturation region. Also derive expressions for ICMR (input common mode range) for the same circuit for a particular value of V_{DD}. Draw parallel n-channel and p-channel differential stage and write expressions for its ICMR. **07**

(b) Explain working of one of the serial ADCs. **07**

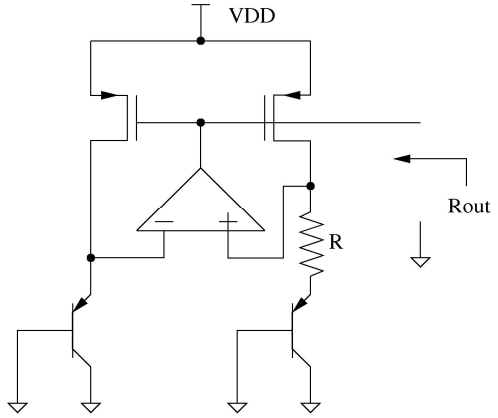

Figure 1: Q:2 (b)

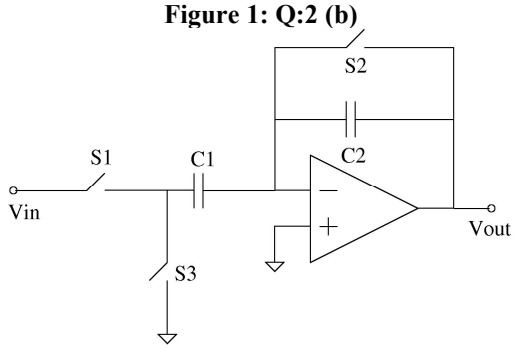

Figure 2 Q:2 (b) OR

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