Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-I Regular Examination January / February 2011

Subject code: 710403N **Subject Name: ASIC Design**

Date: 02 /02 /2011 **Time: 02.30 pm – 05.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as Directed **07**

1 Declare a numeric type called NewINT having range -2 to 6

2 Declare an enumerated data type called VOWEL containing only vowel characters.

3 Declare 4-element array of 8-bit std_logic_vector called array_8.

4 Declare a record called MY_REC having two bytes B0,B1, two integers I0,I1 and two real numbers R0 and R1

5 List the 9 values of std_logic.

6 Declare entity for 4x1 MUX.

7 Define VHDL package.

(b) Write whether following statements are true or false? Justify your answer. **07**

1 The statement a<=b after 5ns in VHDL; is synthesized as a delay line of 5ns.

2 Mealy machine requires more state than Moore machine to do same job.

3 The order of execution of concurrent VHDL statements cannot be predicted.

4 Conditional assignment statements can not be used inside process.

5 Frequency of operation depends on critical path in a circuit.

6 A function can have inout mode parameters.

7 We can not mix structural and dataflow description in the same architecture unit.

Q.2 **(a)** Write short notes on delays in VHDL. **07**

(b) Explain with a neat sketch the architecture of CLB's available in Xilinx FPGA. **07**

OR

(b) With diagram explain FUSE and ANTIFUSE mechanism of FPGA programming. **07**

Q.3 **(a)** Write the VHDL program for 1-bit full adder in all three types of modeling. Also draw the circuit and write truth table. **08**

(b) Write down the truth table and VHDL code for the 4-bit up/down counter. Also draw the circuit and output waveforms **06**

OR

Q.3 **(a)** Write behavioral VHDL code for **08**

(i) 4x1 MUX using with … select construct.

(ii) 1x4 DEMUX using when … else construct.

(b) Write down the truth table and VHDL code for the 4-bit left to right shift register. Also draw the circuit and output waveforms. **06**

Q.4 **(a)** Discuss various loops in VHDL and Explain 'Generate' statement in VHDL with an Example. **07**

(b) Differentiate between a process and wait statement. Can they be used simultaneously in a program? **04**

(c) Explain BLOCK statement. **03**

OR

Q.4 **(a)** Explain the significance of conditional signal assignment statement and selected signal assignment statement with example. **07**

(b) What is the use of Assertion statement? Explain with example. **04**

(c) How will you compare component declaration and component instantiation? **03**

Q.5 **(a)** State diagram of vending machine is shown in figure Q5a below. Write VHDL code using process. **07**

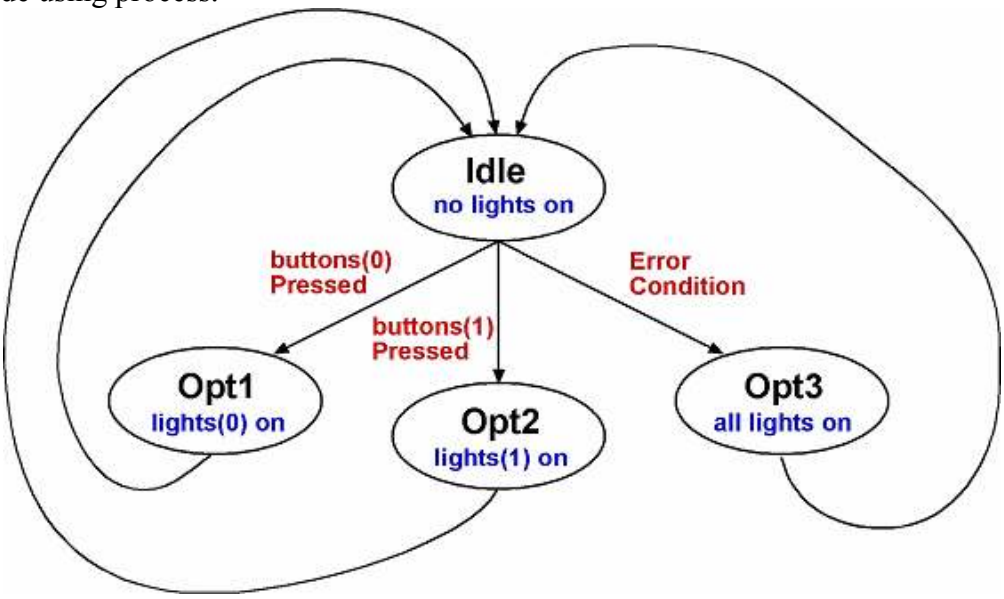

Figure Q5a

(b) For VHDL code shown below, draw circuit in terms of known combinational blocks and flip flops. **07**

```
library ieee;
use ieee.std_logic_1164.all;
entity trans is port
(en,dir: in std_logic;
  a,b: inout std_logic_vector (3 downto 0);
end trans;
architecture con of trans is
begin
Signal temp:std_logic_vector(1 downto 0);
Temp<=(en,dir);
        With temp select
        B<=a when (“11”)
         <=(“zzz”) when others;
        With temp select
        a<=b when (“10”)
         <=(“zzz”) when others;
end con;
```

OR

Q.5 **(a)** Discuss types of FSM (finite state machine) with appropriate example. **07**

(b) For latch shown in figure Q5bor below, write behavioral VHDL code using process. Analyze behavior of the circuit if components U1, U2, U3, U4 are having delay of 5, 10, 10, 6ns respectively. **07**

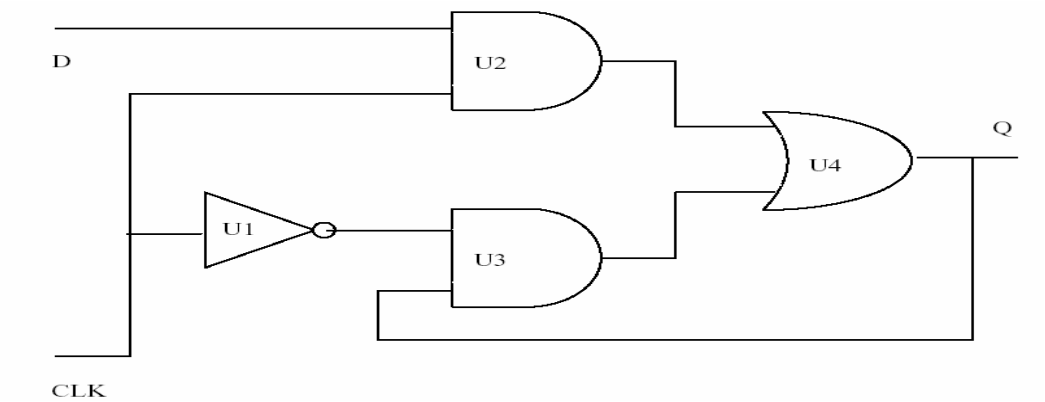

Figure Q5bor

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