Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-I Regular Examination January / February 2011

Subject code: 710412N

Subject Name: Digital VLSI Design

Date: 03 /02 /2011 **Time: 02.30 pm – 05.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Explain with neat sketches wherever necessary.**

Q.1 **(a)** Derive critical voltages for CMOS inverter and find ratio of W/L for symmetrical inverter. **07**

(b) Write short note on CMOS NOR2 Gate. Explain its usefulness. **07**

Q.2 **(a)** Explain in short **07**
(i) Inversion
(ii) Depletion Depth.
(iii) Channel Length Modulation.

(b) Explain two types of scaling with its advantages and disadvantages. **07**

OR

(b) Find the equation for the linear current of MOS structure using GCA. **07**

Q.3 **(a)** Explain typical fabrication process of MOSFET. **07**

(b) Explain device isolation techniques. **07**

OR

Q.3 **(a)** Write detail note on layout design rules for MOSFET. **07**

(b) Write detail note on MOSFET Oxide Capacitances. **07**

Q.4 **(a)** Explain SR latch circuit using sequential MOS logic circuit. **07**

(b) What is Euler path approach? Draw the optimized stick diagram for the following function (CMOS logic), **07**
X= ADF+ B (E+C)

OR

Q.4 **(a)** Discuss the charge sharing problems in VLSI circuit techniques used in domino CMOS circuit for solving charge-sharing problems. **07**

(b) Explain NAND Gate using CMOS, pass and CPL logic. **07**

Q.5 **(a)** Derive expressions for τ_{PHL} and τ_{PLH} using differential equation method. **07**

(b) Consider a CMOS inverter with the following parameters **07**
$V_{TO,n}$=1.0 V $\mu_n C_{ox}$= 45 μA/V^2 $(W/L)_n$=10
$V_{TO,p}$=-1.2 V $\mu_p C_{ox}$=25 μA/V^2 $(W/L)_p$=20
The power supply voltage is 5 V, and output load capacitance is 1.5 pF.
(i) Calculate rise time and fall time using differential equation method.
(ii) Find out maximum frequency of a periodic square-wave input for full 0 to 5 V swing and dynamic power dissipation.

OR

Q.5 **(a)** Write short note on Dynamic CMOS circuit techniques. **07**

(b) Explain in short **07**
(i) Difference between AOI and OAI.
(ii) Difference between Pass and CPL.
(iii) Stick diagram layout of CMOS NOR2.

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