Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-I Regular Examination January / February 2011

Subject code: 712602N

Subject Name: CMOS Circuit Design I

Date: 01 /02 /2011 **Time: 02.30 pm – 05.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** What is the advantage of carry look-ahead adder? Discuss logarithmic look-ahead adder. **07**

(b) Why it is preferred to incorporate NFETs rather than PFETS wherever possible? Discuss MOS device capacitance in detail. **07**

Q.2 **(a)** Draw an active current mirror circuit. Discuss its property and derive small signal gain of the circuit. **07**

(b) In any digital design how power in standby (or sleep) mode is reduced? What is the major advantage of multiple device thresholds? **07**

OR

(b) Discuss the concept of tree and carry save multiplier. **07**

Q.3 **(a)** Describe Manchester Carry-chain Adder with circuit diagram. **07**

(b) How to construct a differential pair whose gain is varied by a control voltage? Discuss Gilbert cell. **07**

OR

Q.3 **(a)** Describe barrel and logarithmic shifter in detail. **07**

(b) 1. Compare performance of various op-amp topologies. **07**
2. Explain power supply rejection in op-amp.

Q.4 **(a)** Derive small signal voltage gain for common-source stage with diode connected load. **07**

(b) For common-source stage with diode connected load calculate the small- signal voltage gain if $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, and ID1=ID2=0.5 mA. What is the gain if M2 is implemented as a diode –connected PMOS device? VDD= |VDS| =3 volt, tox =9 x 10^{-9}, VTO,n=0.7,Lambda,n=0.1,mobility,n=350cm^2/v-s. VTO,p=0.8,Lambda,p=0.2, mobility,p=100 cm^2/v-s, Gamma=0.45, $2\emptyset_F$= 0.9V **07**

OR

Q.4 **(a)** Discuss any one method of Quantitative analysis of differential pair. **07**

(b) Draw the differential pair with small signal inputs. If M2 is twice wide as M1. Calculate the small-signal gain if the bias values of Vin1 and Vin2 are equal. **07**

Q.5 **(a)** Draw Bode plot of loop gain for a two-pole system. Explain slewing in two stage Op-amps. **07**

(b) Write expression for total power consumption in CMOS inverter and explain static power consumption, Dynamic power consumption and direct path power dissipation. **07**

OR

Q.5 **(a)** Discuss performance parameters of an Op-amp. Draw and explain the cascade op amp with input and output shorted. **07**

(b) Discuss frequency response of common source stage amplifier in detail. **07**

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