Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Sem-III Regular Examination January 2011

Subject code: 730406

Subject Name: Peripheral System Design and Interfacing

Date: 10 /01 /2011 **Time: 02.30 pm – 05.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	State and explain different methods for terminating data messages in GPIB bus.	**04**
	(b)	Explain in detail different modes of parallel port in BIOS.	**04**
	(c)	What do you mean by Centronics? Explain Centronics handshaking with timing diagram.	**06**
Q.2	**(a)**	Classify GPIB bus signals and explain all of them in detail.	**07**
	(b)	Explain in detail GPIB (data transfer) handshaking with timing diagram.	**07**
		OR	
	(b)	Explain in detail different GPIB polling methods.	**07**
Q.3	**(a)**	Compare serial and parallel data transfer. State the advantages of serial communication over parallel.	**07**
	(b)	Explain procedure for the parallel port to be used as 8-bits input.	**07**
		OR	
Q.3	**(a)**	State different serial port‘s registers of PCs. Explain any three of them in detail.	**07**
	(b)	Explain in detail ECR with bit assignments w.r.to. parallel port	**07**
Q.4	**(a)**	Explain different program development tools used in µp based system with models.	**07**
	(b)	State different contention schemes in CRT controller. Explain two of them in detail.	**07**
		OR	
Q.4	**(a)**	Explain program development process in detail with flow chart used in µp based system.	**07**
	(b)	What do you mean by frame synchronism using RES? Explain it in detail with timing diagram.	**07**
Q.5	**(a)**	What do you mean by bus? Explain bus structure and bus design in detail.	**07**
	(b)	What is data acquisition system? Draw and explain block diagram of it in detail.	**07**
		OR	
Q.5	**(a)**	Explain in detail EISA, MCA, PCI and VESA VL bus.	**07**
	(b)	Write short notes on “programmable logic controllers”	**07**

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