Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –III Examination Dec. - 2011

Subject code: 732902 **Date: 08/12/2011**

Subject Name: VLSI Circuits and Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Notations/ symbols used have usual meanings.**

Q.1 **(a)** 1. Draw the Y –chart and explain the VLSI design process. **09**
2. What do you mean by hierarchal abstraction?
3. What are the concepts of regularity, modularity and locality?

(b) Illustrate the different operating conditions of the pMOS transistor of enhancement type. **05**

Q.2 **(a)** Derive an equation for saturated drain current considering channel length modulation for MOS transistor. **07**

(b) Draw and explain the different regions for **07**
(i) MOSFET V-I characteristics
(ii) MOS C-V characteristics.

OR

(b) Give comparison for **07**
(i) SRAM –DRAM
(ii) Gate array design –Standard cell based design.

Q.3 **(a)** Along with frequency response, discuss the CMOS amplifier. **06**

(b) Explain the design of **08**
(i) CMOS inverter (ii) Two – input NOR gate.

OR

Q.3 **(a)** What is a CMOS switch? How is it different from the MOS switch? Draw the resistance characteristics of the CMOS switch? **06**

(b) Realize the optimized CMOS logic circuit for **08**

(i) $Y = \overline{A\,(B+C) + DE}$ and (ii)Two input XOR gate.

Q.4 **(a)** Draw the BiCMOS device structure and explain fabrication of same. **07**

(b) Write short note on : ASIC. **07**

OR

Q.4 **(a)** Implement a two – input NOR logic using BiCMOS. **07**

(b) Compare FPGA and CPLD for various aspects. **07**

Q.5 **(a)** Draw the device structure of CMOS inverter. Show the different steps to fabricate a CMOS inverter. **07**

(b) Design a AND latch using TSPC dynamic CMOS logic circuit. **07**

OR

Q.5 **(a)** What is built - in - self test? Explain it with necessary diagrams. **07**

(b) Enlist op-amp's two structures and state its application. Stare design parameters of a CMOS op-amp amplifier and list its various building blocks. **07**

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