Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –II[st] SEMESTER–EXAMINATION – JULY- 2012

Subject code: 1722602 Date: 09/07/2012

Subject Name: CMOS Circuit Design II

Time: 10:30 am – 13:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Show that NMOS and PMOS are poor conductors of '1' and '0', respectively. How can you transmit both levels with same accuracy? What are the precautions to be taken in this new structure of improved switch? **07**

(b) What do you understand by charge injection and clock feedthrough? Explain various charge injection cancellation techniques. Also verify that does it solve the problem of clock feedthrough or not? **07**

Q.2 **(a)** How does the op-amp input offset voltage affect the output voltage in temperature independent voltage reference circuit? What are the solutions to solve this problem? Draw the final circuit which has the less effect of op-amp input offset voltage. **07**

(b) Derive expression for $\Delta V_{BE}/\Delta T$ in voltage reference circuit when variation in I_C w. r. t. temperature is taken into account. What do you understand by PTAT current? **07**

OR

(b) 1. How can you realize a voltage source which has positive temperature coefficient? Justify your answer with necessary mathematical analysis. **07**

2. Discuss the compatibility of implementation of BJT based current/voltage reference circuit in CMOS technology.

Q.3 **(a)** How simple PLL in locked situation does behave in following circumstances? **07**

1. Small transients appearing in input phase
2. Small transients appearing in input frequency

Explain with necessary waveforms.

(b) Draw simple charge pump PLL, explain its working and derive its transfer function. Show that it is unstable. How would you make it stable? **07**

OR

Q.3 **(a)** In implementation of basic charge pump PLL, if there is a time gap of Δt in turning ON of two switches, what could be its effect on control voltage of VCO? How can you avoid this situation? What can be the solution to this problem? Explain with necessary waveforms. **07**

(b) Explain the charge sharing problem which originates due to finite capacitances seen at the drains of current sources in basic charge pump PLL. What is the solution to this problem? Draw necessary circuit schematics and waveforms. **07**

Q.4 **(a)** What are the different issues to be considered in design of sense amplifier? Draw basic sense amplifier circuit and discuss its working. **07**

(b) Draw block diagram of single slope serial ADC and explain its working. **07**

OR

Q.4 **(a)** Draw circuit schematic of sense amplifier which has rail-to-rail input range, minimum kickback noise and "no memory." Discuss its working and justify that it has above mentioned features. **07**

(b) Draw and explain working of charge scaling DACs. **07**

Q.5 **(a)** Explain working of CMOS analog multiplier with necessary mathematical analysis and circuit schematic. **07**

(b) How would you increase the gain bandwidth product of the conventional op-amp? Explain your approach in detail. **07**

OR

Q.5 **(a)** Draw and explain the working of Dickson charge pump. **07**

(b) Which are the two main noise components contributed by MOSFETs? How can we reduce them in MOSFET-based op-amps? List out design techniques for low-noise op-amps. Discuss the significance of low noise op-amps from application point of view. Draw circuit schematic of one of the architectures of low-noise op-amp. **07**

****