Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 1722606 Date: 18/07/2012

Subject Name: Algorithms for VLSI Physical Design Automation

Time: 10:30 am – 13:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	List different layout styles and explain standard cell layout method.	**07**
	(b)	Define circuit partitioning problem. Develop cost function and constraints for the optimization of circuit partitioning.	**07**
Q.2	**(a)**	Enumerate principal differences and similarities between Kernighan-Lin and Fiduccia-Mattheyses heuristics in reference to circuit partitioning problem.	**07**
	(b)	Describe floorplanning model and discuss possible criteria to evaluate quality of floorplans.	**07**
		OR	
	(b)	Categorize floorplanning approaches into three general classes. Explain cluster growth approach for floorplanning.	**07**
Q.3	**(a)**	Discuss min-cut placement algorithm along with its limitations.	**07**
	(b)	How artificial neural network can be used for placement problem? Discuss in detail.	**07**
		OR	
Q.3	**(a)**	What are the factors which decide cost function for placement algorithm? Explain various approaches available for estimation of wirelength.	**07**
	(b)	What is the principal idea behind force-directed placement method? Explain algorithm in brief.	**07**
Q.4	**(a)**	Define routing problem and describe Hadlock's algorithm for speed improvement in routing task.	**07**
	(b)	What do you understand by global routing? Explain sequential global routing approach and Steiner tree problem.	**07**
		OR	
Q.4	**(a)**	Discuss following issues in routing: 1. Multilayer routing, and 2. Power and ground routing.	**07**
	(b)	Discuss application of simulated annealing for global routing problem.	**07**
Q.5	**(a)**	Provide detailed definition of channel routing problem along with cost function.	**07**
	(b)	Discuss the problem of minimizing the layout of a PLA.	**07**
		OR	
Q.5	**(a)**	Explain Dogleg algorithm for channel routing problem.	**07**
	(b)	Discuss optimization of layout generated using gate-matrix methodology.	**07**

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