

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 1724202

Date: 09/07/2012

Subject Name: Testing & Verification of VLSI Design

Time: 10:30 am – 13:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

Q.1 (a) Explain Different Functional Verification Approaches in Detail. **07**

(b) What is the Role of Testing in VLSI Circuit Design explain in detail. **07**

Q.2 (a) List down the Different Types of Testing. Explain Each in Detail **07**

(b) Why Test Data Analysis is Necessary. **07**

OR

(b) Explain the Test Architecture for SOC. **07**

Q.3 (a) Explain Production with reference to test economics. **07**

(b) Explain The Defect Level as a Quality Measure. **07**

OR

Q.3 (a) Explain Different Scan Design Rules. **07**

(b) Explain BITS Pattern Generation. **07**

Q.4 (a) Explain Functional Versus Structural Testing. **07**

(b) Explain the Signal Stuck at Fault. **07**

OR

Q.4 (a) Explain Slow-Clock Combinational test. **07**

(b) Explain I_{DQ} Test Vector Selection from Stuck-Fault Vector Sets. **07**

Q.5 (a) List the Different Types of Simulators Available for Verification. Explain Each in Brief. **07**

(b) What are the Different Verification Strategies? Explain in Detail. **07**

OR

Q.5 (a) Explain different Analog and Mixed Signal Testing Methods. **07**

(b) What are the different ad-hoc methods for DFT. **07**
