Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 1724207 Date: 14/07/2012

Subject Name: Hardware Software Co-Design

Time: 10:30 am – 13:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define Following. 1. Hardware Software Co-Design 2. Modeling 3. Validation 4. Partitioning 5. Scheduling 6. Synthesis 7. Allocation	**07**
	(b)	Explain Co-Design framework and its steps in details.	**07**
Q.2	**(a)**	List the characteristics of a good model.	**07**
	(b)	Describe very clearly the two types of state oriented model.	**07**
		OR	
	(b)	Write a short note on ‘Petri nets”	**07**
Q.3	**(a)**	Explain the difference between state charts and spec charts. Also briefly discuss both.	**07**
	(b)	Give list of various partitioning issues and explain each one of them.	**07**
		OR	
Q.3	**(a)**	Compare VHDL and VERILOG as a specification language.	**07**
	(b)	Compare ‘Structural’ Vs ‘Functional’ Partitioning.	**07**
Q.4	**(a)**	Write a note on Hardware C.	**07**
	(b)	Discuss Instruction Set Architectures.	**07**
		OR	
Q.4	**(a)**	Discuss Instruction Set Processors.	**07**
Q.4	**(b)**	Explain the level of abstraction with reference to HSCD.	**07**
Q.5	**(a)**	Explain RISC and CISC & compare it.	**07**
	(b)	Where does the structure oriented model is required? What is its specialty?	**07**
		OR	
Q.5	**(a)**	Explain Vector Machine and VLIW architecture.	**07**
	(b)	Explain ‘capture & simulate’ and ‘design & synthesis’ very clearly with their advantage and disadvantage.	**07**

****