Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –Ist SEMESTER–EXAMINATION – JULY- 2012

Subject code: 710403N Date: 09/07/2012

Subject Name: ASIC Design

Time: 2:30 pm – 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Give answer of following questions. **07**

(i) List the major capabilities of VHDL along with the features that differentiate it from other hardware description languages.

(ii) Explain VHDL terms: Configuration, Package, Generic and Process.

(b) Write True or False. If statement is true justify it and if false correct it. **07**

(i) The order of execution of concurrent VHDL statements cannot be predicted.

(ii) The statement a<=b after 5 ns; is synthesized as a delay line of 5 ns.

(iii) One entity may be assigned to many architecture bodies.

(iv) We cannot mix structural and data flow description in the same architecture unit.

(v) Structural style is closer to human thinking than behavioral style.

(vi) Every signal in a sensitivity list of a statement must change to fire the statement.

(vii) RTL style describes combinational logic.

Q.2 **(a)** Give answer of following questions. **07**

(i) Compare Inertial and Transport delay with suitable examples and explain Inertial Delay Model.

(ii) What is Delta-delay? What is its effect in VHDL?

(b) Discuss VLSI design methodology. Distinguish between top - down and bottom - up design methodologies for digital design. **07**

OR

(b) Explain the ASIC Design flow in brief. Also explain Full custom and Semi custom mask layout. **07**

Q.3 **(a)** Give answer of following questions. **07**

(i) Which of the followings are VHDL basic identifiers? Which are reserved words?

last_item	prev item	value 1	buffer
element#	_control	93_999	entry_

(ii) Differentiate between concurrent and sequential signal assignment statement. State concurrent assignment problem.

(b) Write VHDL code using behavioral modeling along with test bench for a positive edge-triggered D flip-flop entity. The description should be based on a procedure declared in a package. The procedure has the following signals: **07**

Signal	Mode	Type
d	IN	std logic
clk	IN	std logic
q	OUT	std logic

OR

Q.3 **(a)** Explain data types used in VHDL. List all possible level that can be assigned to std_logic data type. **07**

(b) Design an N-bit parity generator using an XOR gate in a generate statement. Value of N should be passed as a generic parameter with a default value of 8. Use structural modeling style. **07**

Q.4 **(a)** Summarize VHDL attributes. What is the use of FOREIGN attribute in VHDL? **07**

(b) Write VHDL code for a priority encoder using **07**

(i) Conditional assignment statement

(ii) Selected assignment statement

Use dataflow style of description.

OR

Q.4 **(a)** Give answer of following questions. **07**

(i) Write a VHDL code to generate clock with ON period of 15 ns and OFF period of 25 ns.

(ii) Define function overloading & operator overloading.

(b) Write VHDL code for 1K X 8 RAM with separate input and output buses. **07**

Q.5 **(a)** Explain modeling of finite state machines. Also compare Moore state machines and Mealy state machines. **07**

(b) Write the code for an 8-bit Mobius counter. It is an 8-bit shift register where the bits 0 and 1 are XOR'ed and fed to the left serial input at the bit 7. The reset signal should initialize the counter to any state other than "0000". Verify that counter cycles through 15 states and then returns to the initial state. Create a test bench which directly instantiates this counter and generate clock and reset signals. **07**

OR

Q.5 **(a)** Discuss Programmable Logic Devices (PLDs). Also compare CPLD and FPGA. **07**

(b) Give answer of following questions. **07**

(i) How to write a test bench? Give typical test bench format.

(ii) Discuss floor planning and placement.

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