Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –Ist SEMESTER–EXAMINATION – JULY- 2012

Subject code: 710412N Date: 11/07/2012

Subject Name: Digital VLSI Design

Time: 2:30 pm – 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Draw necessary neat sketch wherever necessary.**

Q.1 **(a)** Explain following process for VLSI fabrication with figures. **07**
(i) Oxidation (ii) Photolithography

(b) Discuss the each three domain of Y-chart in detail. **07**

Q.2 **(a)** Describe important criteria to maintain design quality of VLSI. **07**

(b) Explain flat-band voltage in terms of MOS structure with necessary energy band diagrams. **07**

OR

(b) What is threshold voltage of MOS transistor. Describe the four physical component of threshold voltage. **07**

Q.3 **(a)** Describe Accumulation, Depletion and Inversion process for the MOS system under external bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion. **07**

(b) Write short note on voltage Boot-strapping circuit. **07**

OR

Q.3 **(a)** Derive the equation of Drain current (I_D) for an N-channel MOSFET operating in a linear region. Draw the necessary sketch. **07**

(b) CMOS Transmission gate (A short note). **07**

Q.4 **(a)** For a resistive load inverter with V_{DD} = 5V , $k_n^{'}$=20μA/V^2 , V_{T0} = 0.8 V, R_L = 200KΩ, and W/L = 2, Calculate the critical voltages on VTC and draw. Also find Noise Margin of the circuit. **07**

(b) What is clock skew problem for NP-Domino CMOS Logic circuits. Explain True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits. **07**

OR

Q.4 **(a)** Derive the switching threshold (V_{th}) for CMOS inverter. Also prove that for symmetric inverter $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$. **07**

(b) Write a short note on Pre-discharge and Evaluate logic for dynamic logic circuits. **07**

Q.5 **(a)** Explain N-well process. **07**

(b) Short note on FPGA. **07**

OR

Q.5 **(a)** Define delay time definitions for a CMOS inverter. **07**

(b) Short note on CPLD. **07**

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