Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E –IIst SEMESTER–EXAMINATION – JULY- 2012

Subject code: 725203 Date: 10/07/2012

Subject Name: Analog and Mixed Signal IC Design

Time: 10:30 am – 13:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the terms short channel modulation factor and body factor for a MOSFET.	**06**
	(b)	Draw and explain the small signal equivalent circuit of a MOSFET taking into consideration the body effect	**08**
Q.2	**(a)**	Draw the high frequency equivalent of a common source amplifier with current source load. Discuss the frequency response of the amplifier.	**07**
	(b)	What are the different feedback topologies that are used in feedback amplifiers?	**07**
		OR	
	(b)	What are the different noise sources that are present in a common source (CS) amplifier? What is the input referred noise for a CS amplifier?	**07**
Q.3	**(a)**	Draw the circuit diagram of a two stage operational amplifier and explain the operation. What is the gain of the amplifier?	**09**
	(b)	What is offset in opamps? What is the condition for zero offset in a two stage opamp?	**05**
		OR	
Q.3	**(a)**	Explain what is meant by gain boosting in opamps and how it is achieved.	**07**
	(b)	What is common mode feed back in fully differential opamps? Explain the need for common mode feed back in opamps.	**07**
Q.4	**(a)**	Explain what is meant by supply independent biasing. Draw and explain a simple scheme for generating supply independent bias.	**07**
	(b)	Explain what is meant by proportional to absolute temperature (PTAT) voltage. Explain a scheme that generates the PTAT voltage.	**07**
		OR	
Q.4	**(a)**	What are the different building blocks that are required for constructing switch capacitor circuits? Explain with details.	**07**
	(b)	Draw the circuit diagram of a non inverting switched cap amplifier and explain its operation.	**07**
Q.5	**(a)**	Draw and explain the basic architecture of a phase locked loop. Explain the operation of a EXOR circuit as a phase detector.	**07**
	(b)	Draw the circuit diagram of a delay locked loop and explain its operation. What is the application of a DLL?	**07**
		OR	
Q.5	**(a)**	Explain what is meant by quantization noise in analog to digital converters. Obtain expression for the rms value of quantization noise for an ADC.	**07**
	(b)	Draw the circuit diagram of a decoder based DAC and explain its operation.	**07**

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