Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E -IVth SEMESTER–EXAMINATION – MAY- 2012

Subject code: 742601 Date: 12/05/2012

Subject Name: VLSI Test Principles and Architectures

Time: 02:30 pm – 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	List out different types of fault models. Explain stuck-at-faults with the help of half adder circuit. Determine number of collapsed faults for the same circuit.	**07**
	(b)	Define or briefly explain following terms: 1. System availability, 2. Yield, 3. Reject Rate, 4. Design for testability, 5. Fault coverage, 6. Fault detection efficiency, and 7. Transient power supply testing.	**07**
Q.2	**(a)**	Discuss probability-based testability analysis and determine probability-based measures for four-input AND gate.	**07**
	(b)	Draw and explain snap-shot scan design architecture.	**07**
		OR	
	(b)	Define soft error and explain scan-cell design technique which reduces the impact of soft errors.	**07**
Q.3	**(a)**	What are the differences between logic simulation and fault simulation? Explain compiled-code simulation with complete explanation of logic levelization step.	**07**
	(b)	Explain parallel pattern fault simulation (PPFS) with the help of some example circuit. List merits and demerits of PPFS.	**07**
		OR	
Q.3	**(a)**	What do you understand by hazards? What are the different types of hazards? How would you detect hazards without correct delay information (explain in detail with example)?	**07**
	(b)	Write and discuss equations for fault list propagation in deductive fault simulation. Explain deductive fault simulation using circuit of your choice and for one test pattern.	**07**
Q.4	**(a)**	Discuss D-algorithm which is used to generate vectors in combinational circuits (No need to give Pseudo code).	**07**
	(b)	How does sequential ATPG differs from combinational ATPG? Explain the concept of time frame expansion in sequential ATPG.	**07**
		OR	
Q.4	**(a)**	Explain PODEM algorithm (No need to separately write Pseudo codes).	**07**
	(b)	What do you understand by untestable faults? Discuss untestable fault identification.	**07**
Q.5	**(a)**	List out BIST design rules. Explain five of them in detail.	**07**
	(b)	Which are the different fault coverage enhancement approaches? Explain mixed-mode BIST approach in detail.	**07**
		OR	
Q.5	**(a)**	Discuss test pattern generation techniques for exhaustive testing in BIST logic application circuits.	**07**
	(b)	What do you understand by intra- and inter-clock-domain faults? Explain skewed-load approaches for testing multiple clock domain circuits.	**07**

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