Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2013

Subject code: 1724202 Date: 31-05-2013

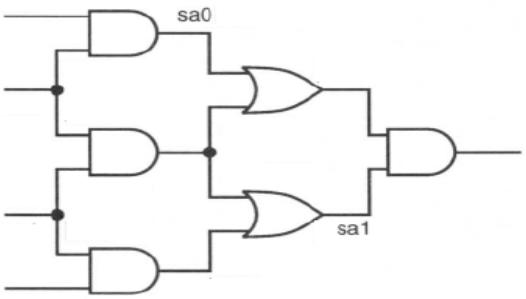
Subject Name: Testing and Verification of VLSI Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Write a test bench for 4 to 1 MUX.	**07**
	(b)	Justify significance of code coverage and functional coverage.	**07**
Q.2	**(a)**	Describe the need for scan chain and explain how it will be implemented?	**07**
	(b)	Write in Brief: i) Design for verification ii)Verification Reuse.	**07**
		OR	
	(b)	Write in Brief: i) Reconvergence model ii) Verification of reusable components.	**07**
Q.3	**(a)**	Explain various verification methodologies. Which verification methodology you will choose after clock tree insertion?	**07**
	(b)	Writ the difference between i) Simulator and emulator ii) Third Party Model and Hardware modeler iii) Cycle based and event Driven Simulation	**07**
		OR	
Q.3	**(a)**	Explain In Brief: i) Fault Equivalence ii) Controllability iii) Observabillity iv) Fault Masking v) Redundant fault vi) Pattern Sensitive Fault vii) On line testing	**07**
	(b)	i) Why fault modeling at logical level is more preferred? ii) Though test generation of multiple faults is possible why it is not attempted commonly?	**07**
Q.4	**(a)**	Explain the stuck open fault for transistor with necessary example.	**07**
	(b)	For a CMOS implementation of NAND gate find out the complete test vector set for all the transistors are stuck open or stuck short.	**07**
		OR	
Q.4	**(a)**	For a gate level implementation given below Find out i) Total number of faults ii) Apply fault dominance and fault equivalence and find out fault collapsing ratio. iii) list out the test set for faults shown in fig.	**07**



(b) For a gate level implementation of XOR gate only using NAND gate **07**
i) Calculate controllability at each net of the implementation
ii) Find out Observability at each net.

Q.5 **(a)** List out various adhoc DFT techniques and explain any two of them in brief. **07**
(b) Explain concept of random access scan. **07**

OR

Q.5 **(a)** What if roll of LFSR in Bist? **07**

(b) What is the significance of ATPG? **07**

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