Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2013

Subject code: 1724205 Date: 05-06-2013

Subject Name: Analog and Mixed Signal VLSI Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Draw small signal equivalent circuit of cascode amplifier and derive the formula of voltage gain, output resistance and -3dB bandwidth. **07**

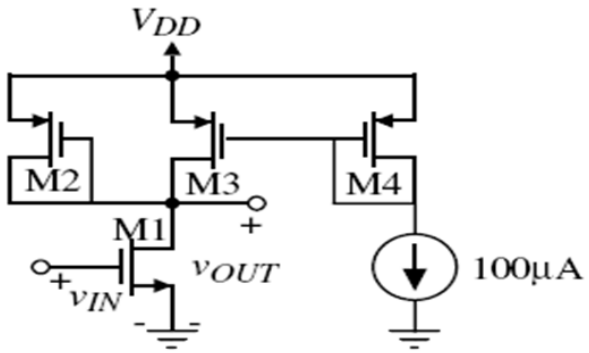
(b) Using the small signal diagram derive the voltage gain and -3dB frequency of Active pMOS load inverter **07**

Q.2 **(a)** Explain MOSFET-Only Voltage Divider. **07**

(b) Explain the significance of class AB CMOS amplifier. **07**

OR

(b) Assume that W/L ratios of Circuit shown in Fig. are $W_1/L_1 = 2\varepsilon m/1\varepsilon m$ and $W_2/L_2 = W_3/L_3 = W_4/L_4 = 1\varepsilon m/1\varepsilon m$. Find the dc value of V_{in} that will give a dc current in M1 of $110\varepsilon A$. Calculate the small signal voltage gain and output resistance. **07**



Q.3 **(a)** Explain Diode Reference Self Biasing. **07**

(b) Explain Two Stage Op-Amp and the significance of compensation in Op-Amp. **07**

OR

Q.3 **(a)** Explain Analog Multiplier in detail. **07**

(b) Explain in detail R-2R DAC Architecture. **07**

Q.4 **(a)** Explain Differential amplifier with current mirror load. **07**

(b) Explain the significance of transistor matching in case of current mirror and discuss different layout techniques. **07**

OR

Q.4 **(a)** Discuss Differential Non-linearity and Integral non-linearity for DAC. **07**

(b) Discuss Current Steering DAC. **07**

Q.5 **(a)** Explain in detail Sense Amplifier. **07**

(b) Explain the working of Pipelined ADC. **07**

OR

Q.5 **(a)** Discussed Phased Frequency Detector. **07**

(b) What is oversampling? Explain Sigma Delta ADC. **07**

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Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage ($V_{BS} = 0$)	0.7 ± 0.15	-0.7 ± 0.15	V
K'	Transconductance parameter (in saturation)	$110.0 \pm 10\%$	$50.0 \pm 10\%$	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 ($L = 1$ μm) 0.01 ($L = 2$ μm)	0.05 ($L = 1$ μm) 0.01 ($L = 2$ μm)	V^{-1}
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V