Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2013

Subject code: 1724207 Date: 07-06-2013

Subject Name: Hardware Software Co-Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Briefly explain the typical Codesign process.	**07**
	(b)	Hardware Software Co Design plays an important role in the field of engineering. Discuss it.	**07**
Q.2	**(a)**	Briefly discuss the level of abstraction with reference to HSCD.	**07**
	(b)	What are the differences between state charts and spec charts? Explain any one.	**07**
		OR	
	(b)	Compare VHDL & Verilog.	**07**
Q.3	**(a)**	How state machine model helps to design three floor elevators? Discuss it.	**07**
	(b)	Write a note on state oriented models and compare it.	**07**
		OR	
Q.3	**(a)**	Discuss Queuing models.	**07**
	(b)	Explain ‘Capture & Simulate’ and ‘Design & Synthesize’.	**07**
Q.4	**(a)**	Write a note on VLIW architecture.	**07**
	(b)	Briefly discuss data driven concurrency.	**07**
		OR	
Q.4	**(a)**	Write a note on SDL.	**07**
	(b)	Explain the difference between functional and structural partitioning.	**07**
Q.5	**(a)**	Discuss partitioning issues.	**07**
	(b)	Explain simulated annealing algorithm.	**07**
		OR	
Q.5	**(a)**	Explain Accuracy Vs Speed in terms of estimation issues. Also explain fidelity.	**07**
	(b)	Define following. a. Hardware programmability b. FPGA c. Modeling d. Validation e. Scheduling	**07**

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