Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

Subject code: 710403N **Date: 13-06-2013**

Subject Name: ASIC Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is ASIC? Draw and explain ASIC design flow.	**07**
	(b)	1) What is Test bench? Write typical test bench format. 2) List different abstraction level of Digital design. Also give difference between top-bottom and bottom-top methodologies for digital design.	**07**
Q.2	**(a)**	What is VHDL? List major capabilities of VHDL along with the features that differentiate it from other hardware description languages.	**07**
	(b)	Explain following terms with reference to VHDL 1) Alias 2) Delta delay 3) Package 4) Generate statement 5) Variable 6) signal 7) Wait statement	**07**
		OR	
	(b)	Explain transport delay model and inertial delay model. Also give comparison between them.	**07**
Q.3	**(a)**	Explain Behavioral Model of VHDL. Also Write VHDL code for 8 bit Magnitude Comparator using behavioral Model	**07**
	(b)	Explain Structural Model of VHDL. Also Write VHDL code for JK Flip flops using any one Model of VHDL. Also write VHDL code for Master-slave JK flip flop using Structural Model of VHDL in which this JK flip flop is used as a component.	**07**
		OR	
Q.3	**(a)**	Draw logic diagram of 1 X 4 DEMUX and write truth table for it. Write VHDL Code for 1 X 4 DEMUX using 1) WITH/SELECT/WHEN statement 2) Case statement	**07**
	(b)	Draw truth table for 8 X 3 encoder. Write VHDL code for 8 X 3 encoder Using: 1. If statement 2. When/else statement	**07**
Q.4	**(a)**	Give difference between Moore FSM and Mealy FSM. Draw Moore FSM for BCD counter. Also write VHDL code for BCD Counter using Moore FSM model.	**07**
	(b)	Write VHDL code for 1101 sequence detector.	**07**
		OR	
Q.4	**(a)**	Explain if-generate statement. Also write VHDL code for 4- bit counter using if-generate statement.	**07**
Q.4	**(b)**	Write VHDL code for 1024 X 8 bit RAM with bidirectional in/out data bus.	**07**
Q.5	**(a)**	What is CPLD? Draw and explain CPLD Architecture.	**07**
	(b)	Explain Programmable Logic devices. Also Give Comparison between PAL, PLA, CPLD and FPGA.	**07**
		OR	
Q.5	**(a)**	Write short note on floor planning and Placement.	**07**
	(b)	What is FPGA? Explain Different types of FPGA.	**07**

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