Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

Subject code: 715202 Date: 04-06-2013

Subject Name: Digital VLSI Design I-Frontend

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain the following in brief: **07**

(1) Mooreôs Law
(2) Yield
(3) Goal of verification
(4) Compare simulation and verification
(5) Clock skew
(6) Partitioning
(7) Shift operators in verilog

(b) Draw ASIC design flow and explain it in detail. **07**

Q.2 **(a)** List various Microscopic issues and Macroscopic issues in design challenges. Explain one issue in each type. **07**

(b) Explain the following in brief: **07**

(1) Floorplanning
(2) Need for testing
(3) Regularity
(4) Modularity
(5) Nonrecurring Engineering (NRE) cost
(6) Bottom-up design
(7) Bitwise operators in verilog

OR

(b) What is the role of ñPortsò in verilog design? Discuss Port declaration and port connection rule. How to connect ports to the external signal? **07**

Q.3 **(a)** Discuss sea of gates and gate array design. **07**

(b) Write a Verilog code for an 8 x 3 encoder. Develop directed and random test bench for the same. **07**

OR

Q.3 **(a)** List various design challenges in sub nano meter design and explain any three in detail. **07**

(b) What is functional verification? Discuss Black-box, white-box and grey-box verification. **07**

Q.4 **(a)** List various data types in verilog and briefly describe any two in detail. **07**

(b) Draw full subtractor circuit diagram, write truth table and Verilog code for the design. **07**

OR

Q.4 **(a)** Define Set-up time and Hold time in digital design. Explain set-up violation and hold violation. **07**

(b) Draw 4-bit Magnitude comparator circuit diagram ,write truth table and Verilog code for the design **07**

Q.5	**(a)**	Compare Mealy and Moore state machine. Design a Moore FSM for the sequence 1011. Draw the state transition table, state transition diagram and signal descriptions.	**07**
	(b)	For the above FSM, write the Verilog code and complete system Verilog test bench.	**07**

OR

Q.5	**(a)**	Design a simple mealy FSM for the sequence 101. Write the Verilog code for the FSM.	**07**
	(b)	Draw and discus Design Hierarchy in HDL language.	**07**

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