Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1724202 Date: 18-06-2014

Subject Name: Testing and Verification of VLSI Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the importanceôs of verification.	**07**
	(b)	What are the different types of coverage? Explain each with necessary examples.	**07**
Q.2	**(a)**	Discuss verification versus testing.	**07**
	(b)	Discuss on Problems for Design Reuse?	**07**
		OR	
	(b)	Give the comparison between third party model and hardware modeler.	**07**
Q.3	**(a)**	Explain the scan based testing.	**07**
	(b)	Explain the TYPE I and TYPE II mistake with reference to verification.	**07**
		OR	
Q.3	**(a)**	What is the use of wave form viewer? What are the limitations of wave form viewer?	**07**
	(b)	With suitable example explain the single stuck-at fault theory.	**07**
Q.4	**(a)**	Describe the Test bench generation process.	**07**
	(b)	Explain the following terms. I. Testability. II. Controllability. III. Observability.	**07**
		OR	
Q.4	**(a)**	Implement the two input NAND gate with CMOS inverter and find out the complete test vector set for all the transistors are stuck open or stuck short.	**07**
	(b)	What is the difference between online BIST and Offline BIST.? Explain the ATPG in brief.	**07**
Q.5	**(a)**	Discuss on VLSI technology trend ñIncreasing transistor Densityò.	**07**
	(b)	Explain the conflicting requirements of go/no-go testing.	**07**
		OR	
Q.5	**(a)**	Explain the Cycle-Free Circuits with example.	**07**
	(b)	Explain Bridging Faults and State Coupling Faults.	**07**

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