Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–I • EXAM – SUMMER 2014

Subject Code: 2715204 Date: 10/06/2014

Subject Name: Digital VLSI Design & Verification- I Frontend

Time:2:30 to 5:30 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** What is the difference between synthesizable and non-synthesizable IP cores? How do Synthesis tools treat the non-synthesizable IP cores? **07**

(b) **07**

```
process(a, b, code)
begin
  if enable = '1' then
    case code is
      when "000" =>
            out <= a + out;
      when "001" =>
            out <= a or b;
      when "100" =>
            out <= a and b;
      when "110" =>
            out <= a - 1;
      when others =>
            null;
    end case;
  end if;
end process;
```

There are multiple problems associated with above code from synthesis point of view. Explain in not more than 5 sentences and suggest corrections in the code.

Q.2 **(a)** What is physical synthesis? In what way, physical synthesis gives better results? **07**

(b) For the given code, **07**

```
module reg_test(clk, in1, out1);
input clk, inp1;
output out1;
reg reg1, reg2, reg3, out1;
  always @ (posedge clk)
  begin
     reg2 = reg1;
     reg1 <= in1;
     reg3 <= reg2;
     out1 = reg3;
  end
endmodule
```

What will be the synthesis output?

OR

(b) What are registered outputs? What is the impact of registered outputs on timing performance of the circuit? **07**

Q.3	**(a)**	Design a state machine to detect sequence 110 if and only if the circuit detected a sequence of 101 anytime within 4 clock cycles before the required sequence. Assume input bit width of three bits per clock. Use Moore machine style.	**07**
	(b)	Modify the state machine in Q3 (a) to count number of times the sequence (110 followed by 101) was detected. Use 5-bit counter. The counter should work as follows: If sequence 110 is detected along with sequence 101 as explained in Q3 (a), the counter should count up. However, if sequence 101 is also detected within four clocks after above sequences are detected; the counter is not to be incremented.	**07**

OR

Q.3	**(a)**	Explain with respect to ASIC design flow, what is clock tree insertion. What are different ways of clock routing structures?	**07**
	(b)	What is the difference between clock skew and clock jitter? How to eliminate clock skew in an FPGA?	**07**
Q.4	**(a)**	Design a synchronous FIFO with 16x8 size with programmable read pointer.	**07**
	(b)	Replicate FIFO designed in Q4 (a) and instantiate two of them in a new design. These FIFOs are now connected to two independent communication channels receiving a byte every clock cycle each. The system should now detect a predefined value 11011110 stored in the FIFO on read side of the FIFO. The two FIFOs may receive this value at different clock times. Whenever both the FIFOs subsequently receive this value, you have to modify the read pointers to match the pointer value at which both FIFOs received the value 11011110.	**07**

OR

Q.4	**(a)**	Explain with suitable timing equations, how to calculate setup and hold slack in a digital circuit. Clearly show all the timing parameters with suitable example and figures.	**07**
	(b)	What is the difference between code coverage and condition coverage? Also explain the terms conformance testing, regression testing, and corner testing with respect to testing a digital circuit.	**07**
Q.5	**(a)**	Write short note on Assertion based verification. In what way, this method is supported by VHDL, Verilog and System Verilog.	**07**
	(b)	Explain various timing and physical constraints to be applied to a digital circuit.	**07**

OR

Q.5	**(a)**	Write short notes on i. Deep Sub Micron effect ii. Coarse grain Vs. fine grain FPGA architecture	**07**
	(b)	What is metastability resolution time? How is Mean Time Before Failure (MTBF) for synchronisers calculated and discuss circuits that improve MTBF.	**07**

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