

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2014

Subject code: 710403N**Date: 19-06-2014****Subject Name: ACIS Design****Time: 02:30 pm - 05:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Explain the typical ASIC Design flow in detail. 07
 (b) Describe the configurable logic blocks used in Xilinx XC4000. 07
- Q.2** (a) Write about an Anti-fuse and Static RAM programming technologies. 07
 (b) Discuss different object types, data types and predefined operators found in VHDL. 07
- OR**
- (b) Write VHDL listing for 4 – bit binary UP and Down Counter. 07
- Q.3** (a) Explain in brief: (1) Full Custom ASICs, (2) Standard Cell – based ASICs. 07
 (b) What do you mean by a device placement? And list the goals of placement. 07
- OR**
- Q.3** (a) Draw the basic block diagram of XC 9500 CPLD and describe it in detail. 07
 (b) Take suitable example of Mealy machine and create a test bench for it use VHDL. 07
- Q.4** (a) What is the need of the Floor Planning? List the major objectives of the Floor Planning. 07
 (b) Write a note on “Timing Driven Placement”. 07
- OR**
- Q.4** (a) Describe the Altera MAX Timing Model for Local Signals in detail. 07
 (b) Give the design of internal architecture of CLB's of ACT -2 and ACT – 3 for C and S class. 07
- Q.5** (a) Using structural modeling implement following function in VHDL: 07

$$Z = A'B'C + A'C' + B'A + AB + A'$$

 (b) Give generic architecture of following devices: 07
 (1)FPGA, (2) CPLD, (3) PLA, (4) PAL.
- OR**
- Q.5** (a) Describe different delays used in VHDL modeling. 07
 (b) Explain following statements by taking suitable example: 07
 (1) If.....els if
 (2) When.....else
