Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2014

Subject code: 710412N **Date: 30-06-2014**

Subject Name: Digital VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain VLSI design flow with necessary diagrams and explain the concepts of regularity, modularity and locality with suitable example. **07**

(b) Consider a MOS system with the following parameters: **07**
tox =200A^o , ū GC = - 0.85 V, NA= 2*10^{15} cm^{-3}, Qox= q* 2 *10^{11} C/cm^2
1) Determine the threshold voltage V under zero bias at room temperature (T = 300 ^{o}K). Note that Ůox=3.97Ů$_0$ and Ůsi=11.7 Ů$_0$.
2) Determine the type (p-type or n-type) and amount of implant required to change the threshold voltage t0 0.8v.

Q.2 **(a)** Draw energy band diagram of the combined MOS system. Explain MOS system under different external bias voltage with energy band diagram. **07**

(b) Write detail note on layout design rules for MOSFET **07**

OR

(b) Discuss Short channel effect in MOSFET with diagram. **07**

Q.3 **(a)** Find out the equation of critical voltages for Noise Margin for the resistive-load n-channel MOSFET inverter circuit **07**

(b) Calculate critical voltages V_{OL},V_{OH},V_{IL},V_{IH} of a depletion-load NMOS inverter: **07**
VT0 = 1V (enhancement-type),VT0 = -3 V(depletion-type),ɔ= 0.4 V$^{1/2}$, ū F=-0.3V,VDD=5V,(W/L)driver=2,(W/L)load=1/3.
Kn,driverô=kn,loadô=25µA/V^2

OR

Q.3 **(a)** Derive the expression of a threshold voltage for n-channel MOSFET. **07**

(b) Design a resistive-load inverter with R = 1 kq , such that V_{OL} = 0.6 V. **07**
The enhancement-type nMOS driver transistor has the following parameters:
V_{DD}= *5* .0 V, Vto= 1. V, γ= 0.2 V$^{1/2,}$ lambda = 0, $\mu_n c_{ox}$=22µA/V^2
(a) Determine the required aspect ratio, W/L.
(b) Determine *VIL* and *VIH.*
(c) Determine the noise margins.

Q.4 **(a)** Calculate the delay time for CMOS inverter during its low to High transition. **07**

(b) µnCox= 120 µA/V2, µpCox= 30 µA/V2,L=0.6µm for both NMOS and PMOS devices $V_{T0,n}$ =0.8 V, $V_{T0,p}$ = -1.0 V, Wmin = 1.2 µm. **07**
Design a CMOS inverter by determining thr channel widths Wn and Wp of the NMOS and pmos transistors to meet the following performance specification.

- Vth =1.5V for VDD=3V .
- Propogation delay times &PHL Ò 0.2 ns and &PLH Ò 0.15 ns.
- A falling delay of 0.35 ns for an output transition from 2V to 0.5V assuming a combined output load capacitance of 300fF and ideal step input.

OR

Q.4	**(a)**	Write short note on CMOS NOR2 Gate. Explain its usefulness	**07**
	(b)	Draw the circuit diagram of CMOS implementation of D-latch along with the simplified view. Also explain the timing diagram of it.	**07**
Q.5	**(a)**	Discuss cascading problem in dynamic CMOS logic circuit with appropriate diagram.	**07**
	(b)	Explain SR Latch circuit using CMOS NAND2 gates.	**07**
		OR	
Q.5	**(a)**	Answer the following questions	
		(1) Realized following Boolean equation using CMOS transmission gates F=AB+AôCô+ABôC.	**03**
		(2)Draw Six-transistor CMOS transmission gate implementation of the XOR function.	**02**
		(3)Draw two input Multiplexer circuit implementation using CMOS transmission gate.	**02**
	(b)	Explain NORA CMOS logic circuits with example.	**07**

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