Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2014

Subject code: 725201 Date: 16-06-2014

Subject Name: Digital VLSI Design II - Backend

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	Explain VLSI Design cycle in detail.	**07**
	(b)	Explain how to measure interconnect delay using interconnect delay models.	**07**
Q.2	(a)	Write down the effects of Clock tree synthesis.	**07**
	(b)	Write a short note on cross talk and its effect.	**07**
		OR	
	(b)	Write down importance of placement in VLSI Design Cycle.	**07**
Q.3	(a)	Explain Generated and Gated Clocks.	**07**
	(b)	Explain with the help of an example calculation of congestion while doing placement.	**07**
		OR	
Q.3	(a)	Write a short note on power network analysis(PNA).	**07**
	(b)	Explain any one routing technique with the help of an example.	**07**
Q.4	(a)	Write a short note on timing driven placement.	**07**
	(b)	Describe the various options available in congested driven placement.	**07**
		OR	
Q. 4	(a)	Explain concept of floor plan with the help of an example.	**07**
	(b)	Write short note on clock tree synthesis methods.	**07**
Q.5	(a)	How to reduce and correct cross talk problem?	**07**
	(b)	Explain the DRC and LVS rules in physical verification.	**07**
		OR	
Q.5	(a)	Explain various file formats used in VLSI Design flow.	**07**
	(b)	Write a short note on power network synthesis (PNS).	**07**

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