Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 725204 Date: 18-06-2014

Subject Name: Protocols and Interfaces

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	Explain the different classes of parallelism and parallel architecture in brief	**07**
	(b)	List out the performance parameters of a computer system. Explain any two in detail.	**07**
Q.2	(a)	Explain the branching process in microcontroller with the suitable example.	**07**
	(b)	Explain the bus structure in computer system.	**07**
		OR	
	(b)	Define cache memory. Explain the structure of cache memory.	**07**
Q.3	(a)	Define interrupt process. Explain the flow of interrupt execution in microcontroller.	**07**
	(b)	Explain the importance of multicore organization.	**07**
		OR	
Q.3	(a)	Explain the architecture of SRAM in detail with data read and write process.	**07**
	(b)	List out the different type of memory available. Compare them in brief.	**07**
Q.4	(a)	Explain the process of interfacing a display device to microprocessor.	**07**
	(b)	Draw and explain the Von Neumann architecture.	**07**
		OR	
Q. 4	(a)	Explain the concept of Interrupt priorities and arbitration in detail.	**07**
	(b)	Write a short note on IEEE 1394 interface.	**07**
Q.5	(a)	Write a short note on SCSI disk protocol.	**07**
	(b)	Explain the basic features of 802.11x protocol in detail.	**07**
		OR	
Q.5	(a)	Explain the basic architecture of Programmable interrupt controller.	**07**
	(b)	What is pipelining? Explain the importance of pipelining in instruction execution.	**07**

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