Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – IV • EXAMINATION – SUMMER • 2014

Subject code: 742601 Date: 04-06-2014

Subject Name: VLSI Test Principles and Architectures

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw and explain scan design flow.	**07**
	(b)	With the help of example explain transistor faults.	**07**
Q.2	**(a)**	Draw Clocked scan cell design and explain its operation with help of waveforms.	**07**
	(b)	Explain transient power supply current testing method used for digital circuit testing,	**07**
		OR	
	(b)	Discuss SCOAP based testability analysis and determine SCOAP combinational measures for 3 input OR gate.	**07**
Q.3	**(a)**	Discuss the two pass event driven simulation. Explain in detail.	**07**
	(b)	Define Logic Element Evaluation. Explain the difference type of Logic Element Evaluation technique.	**07**
		OR	
Q.3	**(a)**	Discuss the different type of delay used in timing models	**07**
	(b)	Discuss the deductive fault simulation.	**07**
Q.4	**(a)**	Explain Bridging fault ATPG with necessary fault models.	**07**
	(b)	Explain: D frontier and J-frontier with the help of example.	**07**
		OR	
Q.4	**(a)**	Define following:1.Level of confidence 2.Test quality 3.Exhaustive testing 4. Delay defect 5. False path 6.Error 7.Fault coverage	**07**
	(b)	How Genetic algorithm is used for ATPG? Explain in details.	**07**
Q.5	**(a)**	Discuss the Cellular Automata technique for Pseudo-Random Testing.	**07**
	(b)	Explain linear feedback shift register in detail.	**07**
		OR	
Q.5	**(a)**	How would you enhance the fault coverage? Write down three approaches for that.	**07**
	(b)	What is the importance of Test Point Insertion approach? Explain with Example.	**07**

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