Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–IV • EXAMINATION – SUMMER 2013

Subject Code: 742601 Date: 14-05-2013

Subject Name: VLSI Test Principles and Architectures

Time: 10.30 am - 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain various bridging fault models.	**07**
	(b)	Define or briefly explain following terms:1.Reliability 2.Repair time 3.Rule of ten 4.Pattern sensitivity fault 5.Coupling fault 6.Delay fault 7.Exhaustive testing	**07**
Q.2	**(a)**	Draw Edge triggered muxed D scan cell design and explain its operation with help of waveforms.	**07**
	(b)	Discuss probability based testability analysis and determine probility based measures for 3 input OR gate.	**07**
		OR	
	(b**)**	Draw and explain Enhanced Scan Architecture.	**07**
Q.3	**(a)**	Explain the equation of fault list propagation in deductive fault simulation with example.	**07**
	(b)	Define Hazard. List out different type of Hazard. How would you detect hazard? Explain in detail with one example circuit.	**07**
		OR	
Q.3	**(a)**	Discuss the two pass event driven simulation. Explain in detail.	**07**
	(b)	Discuss the Transport Delay, Inertial Delay and wire delay in detail	**07**
Q.4	**(a)**	Why 5 value logic is insufficient in sequential circuit testing? Explain with the example the need for 9 value logic.	**07**
	(b)	Classify Path delay faults.	**07**
		OR	
Q.4	**(a)**	Explain boolean difference method for finding test vector with the help of example.	**07**
	(b)	Explain D Algorithm with the help of example.	**07**
Q.5	**(a)**	Discuss serial signature analysis in detail	**07**
	(b)	List out different technique of test pattern generation. Explain any one in detail.	**07**
		OR	
Q.5	**(a)**	List out the BIST design rules. Discuss in brief.	**07**
	(b)	Explain the Single-capture clocking scheme to test multiple clock domain.	**07**

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