Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. IST Semester–Remedial Examination – July- 2011

Subject code: 710403N

Subject Name: ASIC Design

Date:11/07/2011 **Time: 10:30 am – 01:00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Write VHDL codes using WHEN-ELSE statement for following circuits: **07**

1. 4-to-2 priority encoder
2. Four-bit comparator

(b) Write a VHDL code using behavioral description for four-bit shift register which has following features: 1. Parallel load, 2. Left shift, and 3. Right shift. **07**

Q.2 **(a)** Draw a state diagram for Moore type finite state machine (FSM) which generates output '1' when it receives input '1' on two subsequent clock cycles. Include reset signal which brings FSM to initial state when it goes high. Write VHDL code for this FSM using process statement. **07**

(b) Explain configuration and package declaration statements using necessary examples. **07**

OR

(b) Explain various versions of wait statements. What will be the effect of including 'wait for 0 ns' statement within the middle of process statement which has signal assignments statements before and after this wait statement? Explain with appropriate example. **07**

Q.3 **(a)** Discuss assertion statement and write a VHDL code for rising edge triggered D flip-flop with a check on setup and hold times to demonstrate application of this statement. **07**

(b) List out uses of block statement and explain each of them in detail with appropriate statements. **07**

OR

Q.3 **(a)** Explain inertial and transport delay models with necessary examples. **07**

(b) Demonstrate the use of generic and FOR-LOOP statements by writing a VHDL code for n-input NAND gate. **07**

Q.4 **(a)** Give general structure of writing a test bench in VHDL. Write a test bench to generate D and clock inputs for D flip-flop. Assume VHDL code for D flip-flop is available. How do you limit simulation time? **07**

(b) Draw architecture or block diagram of one of the CPLDs and explain its working. **07**

OR

Q.4 **(a)** Draw architecture or block diagram of one of the FPGAs and explain its working. **07**

(b) Write a VHDL program for n-bit adder using structural description by instantiating one-bit adder circuit. Program for one-bit adder must be given. **07**

Q.5	**(a)**	Draw a flow chart indicating major steps involved in chip design using CAD tools. How is functional simulation different from timing simulation?	**07**
	(b)	Write a behavioral VHDL code for four-bit counter with parallel load. Use INTEGER data type for signals.	**07**

OR

Q.5	**(a)**	Explain following terminologies related chip design using CAD tools: 1. Technology mapping, 2. Placement, and 3. Routing.	**07**
	(b)	Write a behavioral VHDL code for two-digit BCD counter.	**07**

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