Seat No.:	Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER - II • EXAMINATION - WINTER 2012

Subje	ect cod	le: 1722901 Date: 29-12-201	2
Subje	ect Na	me: Advanced Power Converters and Control	
		0 am - 01.00 pm Total Marks: 7	0
Instr	uction		
		tempt all questions.	
		ake suitable assumptions wherever necessary. gures to the right indicate full marks.	
	-	otations used have usual meaning.	
Q.1	(a)	Explain series loaded resonant DC-DC converter with discontinuous	07
	(b)	conduction mode. Discuss zero current switch topology for DC-DC buck converter.	07
	(D)	Discuss zero current switch topology for De-De buck converter.	07
Q.2	(a)	Explain in brief, How switching stress can be reduced on Electronics switch using ZCS and ZVS topologies?	07
	(b)	Discuss ZVS clamped voltage topology for DC-DC converter with illustration.	07
	-	OR	
	(b)	Discuss current mode control of DC-DC converter.	07
Q.3	(a)	What are the features of multi-level inverter circuits? Discuss cascaded multi-level inverter circuit.	07
	(b)	Explain diode clamped multi-level inverter with neat diagram. OR	07
Q.3	(a)	Discuss the basic concept of multi pulse converter. Explain how the number of pulses can be increased from available three phase supply.	07
	(b)	Discuss commutation and protection issues related to matrix converters.	07
Q.4	(a) (b)	Explain average modeling of DC-DC buck converter circuit. Explain control characteristics of converters used in HVDC	07 07
	()	transmission system.	
		OR	
Q.4	(a) (b)	Discuss Bi-polar HVDC system along with its merits and demerits. What is need of small signal model? Explain small signal model of converter circuit.	07 07
Q.5	(a)	Write brief note on reactive power drawn by the converters in HVDC system.	07
	(b)	Write brief note on Electronics switches used in matrix converters. OR	07
Q.5	(a)	Explain high frequency link integral half cycle converter with neat diagram.	07
	(b)	Discuss parallel resonant circuit for load resonant inverter.	07
