

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 710403N**Date: 12-01-2013****Subject Name: ASIC Design****Time: 02.30 pm – 05.00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Explain Xilinx 3000 series logic cell with its configurable logic blocks. **07**
(b) Discuss Anti-fuse and Static RAM programming technologies. **07**
- Q.2** (a) What do you understand by Delta – Delay? Also explain Inertial Delay Model and Transport Delay Model. **07**
(b) Describe various Data Types used in VHDL. **07**
OR
(b) Explain various predefined operators in VHDL with their precedence. **07**
- Q.3** (a) What is the need for floor planning and Placement tools? Discuss the core objectives and goals of Floor Planning. **07**
(b) Discuss how the wire – load tables are useful for delay measurement in floorplanning? (Take suitable example if required.) **07**
OR
- Q.3** (a) What are the non-obvious factors that are to be considered for generating pad ring? **07**
(b) Discuss in short : “Timing Driven Placement” **07**
- Q.4** (a) Give the generic architecture for following devices: **07**
CPLD, FPGA, PLA, PAL
(b) Discuss Altera MAX Timing Model for local signals. **07**
OR
- Q.4** (a) Write a note on : Gate-Array-Based ASICs. **07**
(b) Explain the Fish Bone type of clock distribution scheme used for cell – based ASIC. **07**
- Q.5** (a) Using structural modeling write VHDL code to have 4-bit Bit Binary up and down counter. **07**
(b) Write VHDL code to implement the following function: **07**
 $X = ABC + A'B'D' + ABCD + AD' + BC'$
OR
- Q.5** (a) Using with - select - when statement write VHDL code for 4 – bit Parallel Adder **07**
(b) Using case – when statements write VHDL listing for 3X8 Decoder with enable and reset signal facility. **07**
