Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 710412N Date: 17-01-2013

Subject Name: Digital VLSI Design

Time: 02.30 pm – 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain latchup in CMOS circuits.	**07**
	(b)	Explain nMOS transistor in linear region and saturation region.	**07**
Q.2	**(a)**	Expalin two terminal MOS structures.	**07**
	(b)	Explain linear enhancement and depletion load inverter.	**07**
		OR	
	(b)	What is scaling? Explain it.	**07**
Q.3	**(a)**	What is threshold voltage? Explain threshold voltage for MOS transistor.	**07**
	(b)	Explain CMOS inverter.	**07**
		OR	
Q.3	**(a)**	Explain 2 input NOR gate using NMOS and CMOS logic.	**07**
	(b)	Solve Z=[A(D+E)+BE]' using complex logic gate.	**07**
Q.4	**(a)**	Explain 2 stage syncronus complex logic circuit.	**07**
	(b)	What are the layout design rules and explain.	**07**
		OR	
Q.4	**(a)**	Describe the ideal and actual inverter voltage transfer characteristics.	**07**
	(b)	Design 2 input NAND gate using CMOS and pass gate. Also draw layout of 2 input NAND gate.	**07**
Q.5	**(a)**	What is AOI and OAI? Explain AOI and OAI in detail.	**07**
	(b)	Explain NAND base SR latch.	**07**
		OR	
Q.5	**(a)**	Explain static characteristics of CMOS inverter.	**07**
	(b)	Describe the dynamic power dissapation of CMOS inverter.	**07**

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