Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**M. E. - SEMESTER – I • EXAMINATION – WINTER 2012**

**Subject code: 715201 Date: 08/01/2013**

**Subject Name: Semiconductor Device Modeling**

**Time: 02.30 pm – 05.00 pm Total Marks: 70**

## Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | What is trench isolation technique that is used in the present day CMOS processes? Explain how this structure is formed. | **07** |
| | **(b)** | Explain what is meant by channel length modulation in a MOSFET and what is the effect on the IV characteristics of a MOSFET? Give the expression for the drain current in the saturation region with channel length modulation present. | **07** |
| **Q.2** | **(a)** | Draw and explain the band diagrams for a MOS capacitor (diode) made on p type silicon substrate with the bias on the metal electrode varying from a negative value to a large positive value. | **07** |
| | **(b)** | What is photo resist and what is the role of photo resist in VLSI processing. | **07** |
| | | **OR** | |
| | **(b)** | Draw and explain the band diagram of a rectifying and non rectifying metal contacts made on an n type semiconductor. | **07** |
| **Q.3** | **(a)** | Explain the temperature dependence of the resistivity of an extrinsic semiconductor | **07** |
| | **(b)** | What are the four bias modes of operation for a BJT? Compare these four modes of operation. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | What is Fermi energy level in a semiconductor? Explain the dependence of the position of the Fermi level on doping levels. | **07** |
| | **(b)** | What is Early voltage for a BJT? How does it arise and what is the significance of Early voltage. | **07** |
| **Q.4** | **(a)** | Derive the expression for the threshold voltage for a MOS structure made on a p type semiconductor. Assume ideal conditions. | **07** |
| | **(b)** | Draw the band diagrams of a p – n junction diode under zero bias, forward and reverse biases and explain the diagrams. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | What are the triode region and saturation regions of operation for an enhancement MOSFET? Give the expressions for the drain current in these regions and compare the MOSFET operation in these two regions. | **07** |
| | **(b)** | Discuss the behaviour of the threshold voltage for short channel and narrow channel MOSFETs. | **07** |
| **Q.5** | **(a)** | Draw the family characteristics of common emitter and common base configurations and compare them. | **07** |
| | **(b)** | Explain what is meant by self aligned gate and how it is formed. What are the advantages of self aligned gate process. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Describe the importance of oxide layers in VLSI process. What are the various uses that these layers are put to? | **07** |
| | **(b)** | Explain the process of photolithographic image transfer in VLSI processing. | **07** |

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